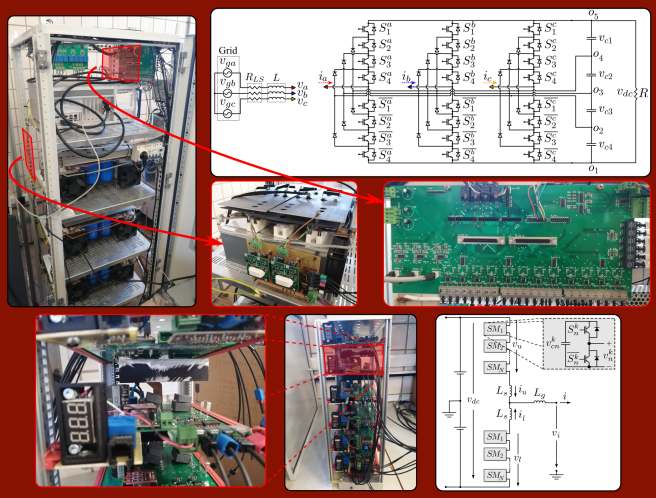
Doctoral Dissertation
Ingeniería Industrial

Contributions to Modulation and Control Algorithms for Multilevel Converters



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Escuela Técnica Superior de Ingeniería
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El tribunal nombrado para juzgar la Tesis arriba indicada, compuesto por los siguientes doctores:

Presidente:

Vocales:

Secretario:

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El Secretario del Tribunal

Fecha:

A Laura
Por su apoyo y empatía en este duro proceso del doctorado. Gracias por inspirarme

A mi familia
Por su apoyo incondicional

A mis amigos
Por soportar llantos y quejas y permitirme disfrutar de su compañía

A mis compañeros de trabajo
Por ser una fuente de inspiración y de apoyo

A mi director
Por su incesante trabajo, esfuerzo y comprensión

Abstract

The current trends on electrical energy have encouraged the search of more efficient systems of generation, distribution and consumption of electrical power. Distributed generation, reduction of passive components, high-voltage DC lines, among others are some lines of research that are being fully considered as the future of electrical grid. This is possible thanks to the advances on the field of power electronics. This work aims at providing a brief glimpse on the current state of power electronics in the field of grid-connected power converters along with some contributions to the control of a particular kind of topologies, referred as multilevel converters, that improve the power conversion efficiency.

It is expected that this work will assist future researchers on setting a framework on the field, and provide them with inspiring material to develop further improvements on the stated solutions.

Contents

Acronyms

AC	Alternating current
ADC	Analog-to-digital converter
APOD-PWM	Alternative phase opposite disposition PWM (type of LS-PWM)
BJT	Bipolar-junction transistors
CART	Classification and regression tree
CB-PWM	Carrier-based pulse-width modulation
CC	Current controller
CHB	Cascaded H-bridge
DC	Direct current
DCC	Diode-clamped converter
DPC	Dierct power control
DTC	Direct torque control
FB	Full-bridge
FC	Flying converter
FCC	Flying capacitor converter
FCS-MPC	Finite-control-set model predictive control
HB	Half-bridge
HDS	Hybrid dynamical system
HV	High-voltage
HVDC	High-voltage direct current
IC	Inner control
IGBT	Insulated-gate-bipolar transistor
LPF	Low-pass filter
LS-PWM	Level-shift PWM
LUT	Look-up table
MICM	Modified integrated control and modulation
MMC	Modular multilevel converter
MPC	Model predictive control

MPC-FCS	Model predictive finite control set
MPP	Maximum power point
MPPT	Maximum power point tracking
MOSFET	Metal-oxide semiconductor field-effect transistor
NLC	Nearest level control
NLM	Nearest level modulation
NPC	Neutral-point clamped
OL	Outer loop
OICM	Original integrated control and modulation
PD-PWM	Phase-disposition PWM
PhDet	Phase detector (used for PLL)
PI	Proportional integral (controller)
PLL	Phase-locked loop
POD-PWM	Phase opposite disposition (type of LS-PWM)
PR	Proportional resonant (controller)
PS-PWM	Phase-shift PWM
PV	Photo-voltaic
PWM	Pulse-width modulation
RMS	Root-mean square
S&H	Sampla & hold
SHE	Selective harmonic elimination
SM	Submodule (for MMC)
SSA	Switching-saving algorithm
SOGI	Second-order general integrator
SV	Space vector
SVBA	Space-vector-based algorithm
SVM	Space-vector modulation
VCO	Voltage controlled oscillator (used for PLL)
VSC	Voltage source converter
VSI	Voltage source inverter
ZOH	Zero-order hold

1 Introduction

If you want to find the secrets of the universe, think in terms of energy, frequency and vibration.

Nikola Tesla

This chapter introduces the basis knowledge and state of art that settled the contributions of this work. For this, a brief glimpse in the field of power electronics is firstly given before entering the main theme of this work, multilevel converters.

It is expected that this chapter helps future researchers to become acquainted with the state-of-art of grid-connected power converters at the moment this work was written, and assists others in the comprehension of power electronics.

In the following, a brief description of the document content is firstly given, along with its objectives and structure. Secondly, a more extended background and state-of-art is provided.

1.1 Document description

1.1.1 Context of the research

This research has been carried out under the following projects:

- *Control no lineal del balance de tensiones en convertidores multinivel (DPI2013-41891-R).*
- *Control de Sistemas con Entradas Discretas. Aplicación a Convertidores Electrónicos de Potencia (DPI2016-75294-C2-1-R).*
- *ECO-MIR: Estabilidad y COntrol no lineal de MIcRorredes (US-1264655).*
- *Problemas de Estabilidad Global en Microrredes (PID2019-109071RB-I00).*

The context of this research is placed within the Power Electronics field, which is the application of solid-state electronic devices to the control and conversion of electrical

energy. Power Electronics field covers from developing solid-state devices, such as insulated gate bipolar transistor (IGBTs) [1]; arranging them into systems that handle the electrical energy, generally power converters [2]; and designing control strategies to fulfill the objectives for which they have been constructed [3].

Power Electronics has widened considerably in the last decades and there are plenty of research currently available. That is why researchers focus on particular features inside this field. Indeed, the work presented in this thesis is aimed to follow the same scheme, and the contributions presented here are narrowed down to the control of certain topologies of power converters. However, in order to provide a proper framework, the second part of this introduction will cover the background of the current work.

Nowadays, the electrical grid uses high-voltage transmission lines to distribute electrical power between distant geographical points. This is so due to the reduced conducting losses that high-voltage transmission lines have in comparison with the low-voltage ones. However, the standard power converters are composed of solid-state devices that do not have the voltage limits high enough to be connected directly to these lines, and therefore an intermediate stage is required to shift the voltage levels, which is usually a transformer device. This solution not only implies additional hardware but also it generates more losses, reducing the overall efficiency of the system. As an alternative [4], the multilevel converter was introduced in the early 90s [5], which overcame the voltage limitations of standard power converters by serializing more than two solid-state devices in such a way that the voltage limits are extended. In this way, the same devices can be used in systems with higher voltage rates without requiring transformers. Additionally, by using several levels, better quality of the phase currents and potential reduction in the filter sizes are achieved. However, due to the increased hardware, the control complexity of the system is also increased. This work aims to present several approaches that overcome this issue.

1.1.2 Objectives

The objectives of this work are the following:

- About the current state-of-art:
  - To present the current state-of-art of grid-connected power converters.
  - To exhibit the basis and foundations of power converters.
  - To explore the typical approaches for controlling multilevel power converters.
- About new contributions:
  - To present some contributions to the control and modulation of multilevel power converters. These contributions have to consider the topology under study, model its desired behaviour and propose an algorithm that covers the control objectives of such stage. Additionally, the proposed algorithms might take into account some performance indicators in order to develop a more optimal solution.
  - To depict the benefits of such novel approaches in comparison with the existing ones. For this, some approaches that are already presented in the literature are

examined and evaluated under the same conditions. In order to depict the benefits some performance indicators are exhibited and used. These comparisons are usually carried out both under simulation and experiments.

1.1.3 Structure

The structure of this work is the following

1. This first chapter (Chap. 1) will exhibit the background, some fundamentals and the current state-of-art of power electronics, power converters and control of grid-connected power converters. An introduction to multilevel power converters is also included: topologies, modulation and approaches without modulation stage.
2. The second chapter (Chap. 2) firstly provides a deeper insight into diode-clamped converters and their principle of operation. Afterwards, the main contributions developed for three-level DCC (Sect. 2.2) and five-level DCC (Sect. 2.3) are presented.
3. The third chapter (Chap. 3) introduces the topologies of cascaded and modular converters along with their principle of operation, differences and similarities. Later on, a contribution for cascaded H-bridge topology (Sect. 3.2) and another one for modular multilevel converter (Sect. 3.3) are presented.
4. Lastly, some conclusions are drawn (Chap. 4) about the particular contributions of this work (Sect. 4.1) and possible future works (Sect. 4.2).

1.1.4 List of Publications

Published works

The following papers and contributions have been published as a result of the current work

[1] P. Montero and F. Gordillo, "A modulation algorithm for inter-phase balancing in CHB Converters," in *2017 11th IEEE International Confer-ence on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, pp. 133–138, IEEE, 2017.

[2] P. Montero-Robina and F. Gordillo, "A Novel Controller for Grid-Interfacing Solar Arrays Through Five-Level Diode-Clamped Converters," in *2018 IEEE 18th International Power Electronics and Motion Control Conference (PEMC2018)*, pp. 955–961, IEEE, Aug. 2018.

[3] P. Montero-Robina, F. Umbria, F. Salas, and F. Gordillo, "Integrated Control of Five-Level Diode-Clamped Rectifiers," *IEEE Transactions on Industrial Electronics*, vol. 66, pp. 6628–6636, Sep. 2019.

[4] P. Montero-Robina and F. Gordillo, "A thermal analysis for two modulation and control approaches for five-level diode-clamped rectifiers," in *IECON2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 2019, pp. 3135–3141, IEEE, Oct. 2019.

[5] P. Montero-Robina, F. Gordillo, F. Gómez-Estern, and F. Salas, "Voltage balance for five-level DCC based on mixed-integer linear programming," *International Journal of Electrical Power & Energy Systems*, vol. 124, p. 106302, Jan. 2021.

Submitted papers

The following papers were submitted at the moment this dissertation was written

[1] P. Montero-Robina, F. Gordillo, F. Cuesta, and F. Gómez-Estern, "Pseudo-optimal Five-Level DCC Modulation Based on Machine Learning," *Submitted to IEEE Transactions on Power Electronics*, Jan. 2021.

[2] P. Montero-Robina, C. Albea, F. Gómez-Estern Aguilar, and F. Gordillo, "Hybrid modelling and control of Three-level NPC Rectifiers," *Submitted to Control Engineering Practice*, May 2021.

[3] P. Montero-Robina, K. Rouzbehi, F. Gordillo, J. Pou, "Voltage Source Converters: Current Control Techniques Operating with Unbalanced Voltage Conditions," *Submitted to IEEE Open Journal of the Industrial Electronics Society*, May 2021.

[4] P. Montero-Robina, A. Marquez, M. S. A. Dahidah, S. Vazquez, J. I. Leon, G. Konstantinou, and L. G. Franquelo, "Feed-forward Modulation Technique for more Accurate Operation of Modular Multilevel Converters," *Submitted to IEEE Transactions on Power Electronics*, May 2021.

1.2 Background and current state-of-art of grid-connected VSC

This section presents the current state-of-art of all fields that constituted the basis from which this dissertation started. They are separated into five subsections that are summarized in the next paragraphs.

Firstly, an introduction in the field of power electronics field is given. Solid-state devices and the most common power converters topologies will be exposed.

The second subsection is devoted to present the general scheme of the electrical grid, its properties and configurations. There are plenty of assumptions throughout this document that are based on particular conditions of the electrical grid, and thus they will be explained in this subsection.

The third subsection exhibits how the power converters are typically controlled. This task generally involves several stages with different control objectives. Besides, the approaches to achieve the power converter control are not unique and their suitability depends on the desired application and performance.

The fourth subsection presents the multilevel converter topology, advantages, challenges, common topologies and trends. Note that this document focuses on researching for this kind of power converters, however not all topologies presented in this chapter will be later studied. They are included to show the reader an insight of the field.

Lastly, the fifth subsection presents some of the most known modulation techniques for multilevel converter, that is, the way that the control input is integrated in the power converter in order to achieve the desired effect. Some of the modulation techniques require to fulfill additional control objectives when used for multilevel converters, and thus they will be exposed here.

1.2.1 Power electronics

A power electronic system generally follows a scheme composed of a power source, a filtering stage, a power converter, a load and a control circuit [6]. The power source could be of any nature and electrical characteristic, and the main objective is to transfer the generated power from the power source to the load as efficiently as possible. The filter stage is in charge of eliminating those undesired components from the power flow, and thus it can be allocated either after the power source, before the load or in both positions using two filtering stages. The power converter is in charge of manipulating the power flow in such a way that it acquires the characteristics that are desired for the load. This task is carried out by using controlled or uncontrolled solid-state devices that compose the power converter. In the case they are controllable, the switching on/off of the devices is governed by a control circuit, which gets information from the source, the load and the power converter to dictate the power converter how to behave. The nature of this control circuit is discrete—as the gating signals are discrete values—and it can be either a digital algorithm with analog-to-digital (ADC) ports for the measurements or an analog controller integrated in a circuit. A scheme of this type of system is depicted in Fig. 1.1.

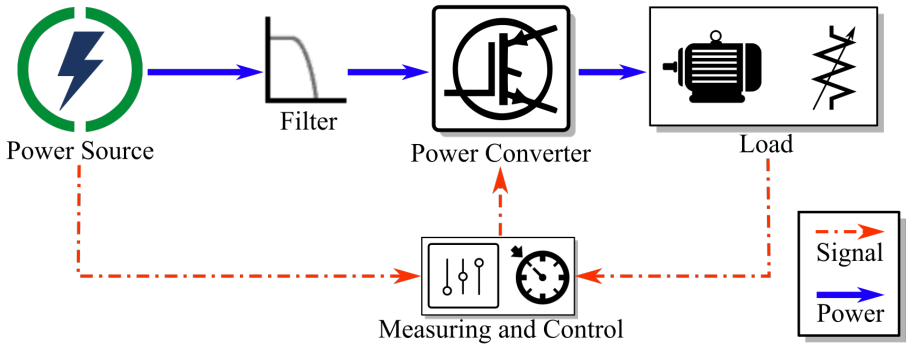

Figure 1.1 Power electronic system scheme.

This work mainly uses the alternating-current (AC) grid as the power source; passive components, such as inductors or capacitors, as filters; controlled power converters with digital controllers; and pure resistive loads. Although, there are some applications that do not follow the same scheme and it will be clarified in those cases.

Solid-state devices

The solid-state devices are named after its property of being a solid material that can change the flow of charges, i.e. allow the electrical current to pass through or not. In contrast to earlier technologies—gas, vacuum or electro-mechanical devices—there is no change of state, nor any movement within the device when this property changes, allowing them to act as fast switching devices [7].

The main solid-state devices that act as power semiconductors are the following:

- Power Diodes

- Thyristors
- Bipolar-junction transistors (BJT)
- Metal-oxide-semiconductor field-effect transistors (MOSFET)
- Insulated-gate-bipolar transistors (IGBT)

Power diodes acts similar to signal diodes but for an increased reverse breakdown voltage and increased forward current capability.

Thyristors cover a wide family of solid-state devices—Silicon-controlled rectifier (SCR), gate turn-off thyristor (GTO), etc.—that share a similar principle of operation: a bistable mode of operation where either they work in conducting state or not. The operability of them changes from one device to another, but they are able to sustain larger amount of voltages and currents than those other switching devices that are fully operable.

BJTs were one of the first fully controllable transistors introduced in the industry whose output current could be controlled from the base. However, the power BJTs have been generally deprecated in power applications by MOSFETs and IGBTs, although there are some applications where BJTs are preferable due to the reduced hardware requirement to switch them, its low cost, its relatively high switching speed, and low switching losses.

Power MOSFETs are voltage-controlled devices whose internal disposition slightly differs from its low-power version, increasing their voltage limits and parasitic resistance at the same time. In comparison with IGBTs, the required driving circuit to switch them is simpler and yields lower switching losses. Additionally, their lower switching delays allows them to reach higher switching frequencies when compared to BJTs or IGBTs.

Lastly, IGBTs are a combination of the BJTs and power MOSFETs that collects the advantages of both. Thus, it is one of the most used solid-state devices in power applications. They have better conduction characteristics and larger voltage and current limits than power MOSFETs but lower dynamics. They are suitable for power applications with lower switching frequencies (< 20 kHz) but larger power magnitudes.

Power converters

Power converters are the circuits that fulfill the power conditioning objectives of the specific application they were designed for. They are composed of solid-state devices that comply with the magnitude limits of the application. Considering that electricity comes in the form of direct-current (DC) or alternating-current (AC), the topologies of power converters are usually classified according to the input-output nature, i.e. AC-AC, AC-DC, DC-AC or DC-DC. Additionally, each of these topologies have particular characteristics that define their performance, for example, whether they require control actions or not, bidirectional power flow capability, single or three-phase mode of operation for AC, interleaving capabilities for DC, etc. There are plenty of topologies and new ones are being released nowadays, short summaries are exposed in [2, 3, 6].

AC-DC Converters:
They subtract power from an AC source to stabilize a DC output voltage. These are very common converters in low-power applications given the fact that the electrical grid is AC while most of the consumer electronics are fed with DC voltages. Additionally, many

power converters for aircraft applications are included in this category, as the energy comes from the varying-speed turbines. AC to DC operation is also referred as rectifier mode of operation, and it is common to refer to unidirectional AC-DC power converters as rectifiers. In this regard, the non-controlled diode-rectifier is the simplest construction, which is made up from power diodes that allow the AC current to pass through only in a certain direction, resulting in a positive current delivery. As a consequence, the filtering stage for it is vital given that the current distortion is high, but it does not require external controller. Additionally, there is no control on the reactive power flow which can further increase the considered losses. It is a solution that prioritize compactness and simplicity over performance.

Nevertheless, there exists solutions that allow certain degree of control, such that SCR-based rectifiers or power factor correction converters (PFC). These solutions vary in the used devices and capabilities, but they allow the system to modify the output DC voltage within a certain range, and handle the reactive power in some cases. It is worth mentioning that the three-phase voltage source converters (VSCs) are one of the most extended and used topologies due to its bidirectional power flow and its capability of achieving high degree of controllability on the system performance.

There is also modular solutions for three-phase applications that consists on combining three single-phase PFCs serialized with a DC-DC converter each, in such a way that each chain contributes to a common DC voltage bus. Alternatively, PFC can be achieved by means of harmonic compensation, which require additional power electronic circuitry to modify the current waveforms.

DC-AC Converters:

The converters inside this category are also known as inverters, which are capable of transforming a DC magnitude into an AC one. Due to the requirements for the AC output, these converters are always controllable and use gate-controlled power switches. The AC output can be of any phase, magnitude and frequency—within the range of operation of the converter—which makes them suitable for injecting power from a DC source to the electrical grid. Indeed, it is very common to use such converters for renewable energy integration or as grid back-ups when there is shortage of energy production in the electrical grid. Similarly to AC-DC, the voltage source inverters (VSI) are the most used ones.

It is very common to catalogue the converter modulation approach inside this topology depending on the type of the AC signal they produce: Square wave, modified square wave and sine wave. For the square wave and modified square wave outputs, the AC signal is produced by using square pulses of the same frequency than the desired AC output, being the filter stage in charge of smoothing out the generated distortion due to this mismatch. In contrast to the simple square wave approach that uses online positive and negative, modified square wave uses positive, zero and negative magnitude pulses, improving the output spectrum quality. Alternatively, thanks to the advancement on power electronics, the so-called true sine wave inverters are possible, which use a modulation technique to generate a more accurate AC signal.

DC-DC Converters:

The converters within this topology transform the DC voltage magnitude from one value to a different one. On the one hand, this kind of converters are used to guarantee a stable DC-voltage at the output, so they have to handle the variations both in the output power

demand and the DC input magnitude. On the other hand, there are applications that require a variable DC output voltage, where the power converter 'chops' the input DC voltage to a lower value, and thus they are usually known as choppers. Nevertheless, power switches are employed to fulfill such purpose [8].

Regarding the classification, they are usually segregated by their capability to output a larger and/or lower voltage magnitude. Besides, along this capability, providing an isolated output or not with respect to the input is another factor to consider.

The fundamental non-isolated DC-DC converters are usually composed of one switching device, one power diode and one or more passive component (inductor or capacitor). Their performance consists on using the switching device to modify the current flow in such a way that its interaction with the passive component and the diode over a period of time modifies the output voltage. Thus, by modifying the time the switch is closed, the output voltage can be modified accordingly. Typical converters in this category are the buck converter (lower output), boost convert (larger output) and buck-boost converter (both options) [9].

Isolated DC-DC converters use an isolation transformer or coupled inductor to generate an output that is electrically isolated from its input. Similarly to the non-isolated version, they rely on a switching device that, commuting at high frequencies, allows to transfer power from one side to another. Again, the interaction of the coupling agent (transformer or coupled inductor) with the switching of the power device(s) is the factor that modifies the output voltage. Some fundamental topologies of isolated DC-DC converters are the flyback converter, the forward converter, the half-bridge converter and the full-bridge converter [10].

AC-AC Converters:
These kind of converters are required in those applications where the power is extracted from an AC source and delivered to another AC system with different characteristics. One flexible way to do so is by using the back-to-back configuration which consists in using an AC-DC connected to a DC-AC converter through the DC stage, usually referred as the dc-link, which contains an energy storage element. These converters can be classified as indirect AC-AC converters with all the properties the involved AC-DC and DC-AC converters have [11]. Nonetheless, there exists one-stage direct AC-AC converters that do not require energy storage elements. The most used ones are the cycloconverter and the matrix converter [12]. The cycloconverters use two controlled rectifiers (composed of SCRs or other kind of thyristors) to modify the injected current in terminals of the load, whereas the matrix converters use $k \times l$ bidirectional switches, such as two IGBTs in antiparallel configuration, to connect a $k-$phase source to a $l-$phase load. Both configurations do not require large storing elements, but cycloconverters can only modify the frequency at the output, while matrix converters can reduce the voltage magnitude and increase the frequency.

1.2.2 Electrical grid

The most basic scheme of the electrical grid is composed of three elements: production, transmission-distribution, and consumption. The characteristics of each element are not unique and they are mainly defined by the scope and context of the actors involved [13].

Up to the date, the grid has been mainly developed in alternating current (AC) being the frequency and amplitude magnitude defined by the geographical region it is implemented. The main reason AC has been selected preferably over DC is due to the fact that stepping up and down the voltage magnitude is straightforward by means of a transformer. However, there are some drawbacks, such as additional losses due to parasitic coupling, undesired electromagnetic emissions, and the appearance of the so-called reactive power. The latter is caused by the presence of current distortion and a phase-shift between the fundamental components of the phase voltage and current, which, over a grid period, yields no energy transmission, but the losses associated to the current still remain.

In terms of structure, it has kept a traditional scheme of a vertical hierarchy in which energy is transferred from large production centers through transmission lines, and then adapted to be distributed among the consumers. Given that the energy production must match the energy consumption, it is necessary to monitor this condition, and thus the more centralized the grid, the easier to control. However, the introduction of distributed energy generation, specially due to renewable energy, and the intermittent consumers have pushed the industry to look for solutions to stabilize the grid conditions [14]. In this regard, load forecasting models, reactive power compensators, flexible AC transmission systems, etc. have been proposed to provide some means to correct deviations in the desired frequency and voltage amplitude [15–17].

Nonetheless, the principle of using high-voltage lines for large transmission kept unchanged. This is due to the fact that conduction losses are proportional to I_{rms}, being I_{rms} the root mean square (RMS) of the current that is transferred. Considering that a transmitted power (p) that is kept constant in a single line is defined by:

$$p = V_{\text{rms}} I_{\text{rms}}, \tag{1.1}$$

where V_{rms} is the RMS voltage of the grid. The larger the V_{rms}, the lower the needed I_{rms} to transfer the same active power, and thus the lower the losses. For this, the common scheme is to step-up the voltage before reaching the transmission line, and consequently the losses are reduced in the transportation process.

Despite the fact that this process is easily achieved by a transformer thanks to the nature of AC, the transformers are bulky, expensive and generate additional losses, although they are largely compensated by the avoided losses involved in the transportation. For this, it is a fact that AC transmission lines have to be operated at high voltages (HV) and later stepped down to distribution and consumer levels. At this point, the question about why generating power at low voltages when they are later required to be increased arises. Indeed, the generation is usually in the low-voltage side due to the limitations of energy generation drives and power semiconductors, where the elements involved cannot stand such a high voltage.

For those cases of large power generation plants, such as nuclear, thermal or hydroelectric, using the transformer seems the most straightforward solution as the generation is very concentrated [18]. However, for distributed generation where lower power sources are geographically spread, using a transformer for each node or gathering all lines into one transformer are economically infeasible solutions. In this context, the concept of multilevel converter arises as a solution that extends the voltage limits of the converter

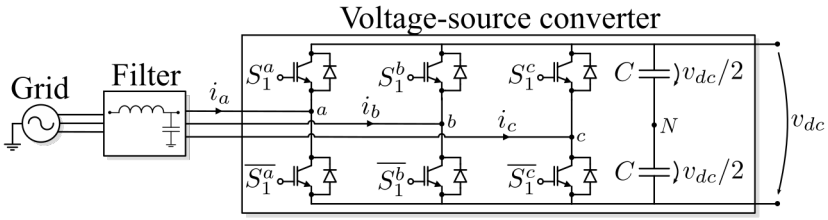

Figure 1.2 Scheme of grid-connected two-level voltage source converter (AC-DC converter).

beyond those of the power devices within it. With this, the necessity of a transformer might be avoided (or replaced by a smaller and cheaper one), and some drives or power sources can be directly connected to higher voltage lines [19–22]. The multilevel converter topology will be explained later in more detail.

Furthermore, there is a new trend towards using high-voltage direct-current lines (HVDC) [23] that keep the advantages of reduced conduction losses, while adding faster dynamics, no electromagnetic emissions, no reactive power and no parasitic capacitance. However, the stepping up and down is not so easily achieved and further research is still being conducted with HVDC lines.

1.2.3 Power converter control

Considering the previous definition, power converters can be seen as autonomous systems, whose performance is defined by the control strategy and the fixed objectives [24]. Note that the control of power converters is a challenging task given that most of the variables that define the system performance are natural and continuous, e.g. currents and voltages, while the control variables are discrete, i.e. the gating signals of the power devices. Besides, some non-controlled semiconductor devices, such as the power diode, does not behave linearly and thus, the modelling of systems that include them is more difficult.

Nevertheless, a common strategy is to use a continuous controller in a closed-loop control where the control signals are transformed from continuous to discrete by means of a modulator, that is, the stage in charge of switching the semiconductor devices according to the control input signals. In this line, for AC-DC converters where the DC voltage magnitude has to be regulated as well as the AC currents, and given that there exists a relation between them, it is common to employ a cascaded control strategy, where one slow-dynamic loop is serialized with the fast-dynamic loop. Nevertheless, there exists some control approaches that do not follow this scheme, skip the modulation stage, or define a control that does not require a cascaded configuration. Given that this work focuses on grid-connected power converters, the fully controllable AC-DC converter with rectifier capabilities depicted in Fig. 1.2 will be considered for the remaining of this section.

Control objectives

The control objectives depend on the application for which the converter under control will be used. Nevertheless, there exists some common objectives commonly accepted [25]:

1. *To reduce losses*: there are conducting and switching losses. The first ones are inherent to the resistive elements within the system and they are proportional to the square of the current magnitude. The second ones are caused by the switching of the semiconductor devices, as there is an associated energy (E_{ON}, E_{OFF}) for each switching action. The first ones can be reduced by limiting as much as possible the AC current magnitudes—by reducing the harmonic content or reactive power—, and the second one must be tackled from the modulator by avoiding unnecessary commutations.
2. *Minimal low-order harmonic content or reduced distortion*: Not only this objective assist on the achievement of the previous objective, but it is also required for grid-connected power converters to attain to the harmonic grid code limits in the AC side. Additionally, some power converter applications aim for reducing the harmonic content in the existing phase currents or DC voltage magnitude, and thus this objective becomes critical. In grid-connected applications, this objective can be applied for both the AC current magnitude or the voltage magnitude at the DC side.
3. *Reduced ripple*: Due to the modulator stage, there is an inherent ripple around the switching frequency and its multiples. This frequency is usually much larger than the fundamental AC frequency (more than 20 times larger), and thus passive filters attenuate its component. Nevertheless, any contribution to the reduction of this ripple would assist on reducing the losses, reducing the required size of the passive components, etc.
4. *Fast response*: Grid-connected power converter applications must response quickly when a sudden change in the power flow is given, otherwise they might fail on sustaining the energy supply.
5. *Zero steady-state error*: For some control problems, achieving this is not a straightforward objective whatsoever. Indeed, some linear controllers can be used to achieve sinusoidal currents, but they do not match the desired current amplitude or phase, and thus they do not achieve zero steady-state error.

Notice that, there are some objectives that can contradict each other, such as reduced ripple and to minimize switching losses, therefore there is a trade-off in the fulfillment of some of these objectives.

Control strategies

When a modulator is used, the classical continuous controllers can be implemented in such a way that they track the averaged values of the system variables (generally current or voltage magnitudes), providing an averaged control signal u. Afterwards, the modulator is used to implement this control signal into the converter, that is, converting the continuous control signal u into a discrete one y. For this, the control signal should be mathematically adapted according to the system dynamic in such a way that the resulting signal is bounded within the region [0,1]. This variable, which is the so-called duty ratio d, is modulated by having the discrete output signal y equal to 1 an averaged time equal to d, and 0 the remaining time. The period over which this signal is averaged is known as the switching

period T_s—inverse of the switching frequency f_s—. In this way, the duty ratio d expresses the amount of time within a switching period T_s that the discrete output signal y is equal to 1. This scheme is also known as pulse-width modulation (PWM) where d represents the width of the pulse that is generated every switching period. For example, using a non-symmetrical pulse generation:

$$\text{every } t \in [0,T_s] : \begin{cases} y & = 1 \text{ for } \quad t < T_{\text{ON}} = dT_s \\ y & = 0 \text{ for } \quad t \geq T_{\text{ON}} \end{cases}. \tag{1.2}$$

Consequently, except for those boundary cases of $d = 0,1$, there will be two commutations per phase every period T_s, which generates a ripple in the modulated system magnitude, fundamentally concentrated around f_s or its multiples. There exists plenty of modulation schemes that will be explained later.

There is another set of control strategies that does not use this common scheme of continuous controller plus a modulator. Instead, they compute the discrete signals straightforwardly, that is, considering all possible combinations of the outputs. In this regard, it is worth mentioning that a standard three-phase two-level AC-DC converter with six power devices has $2^3 = 8$ possible combinations—two positions for each phase—as there are forbidden positions that does not add up to these set of choices. Consequently, the used control scheme can take advantage of this knowledge to select the more appropriate control input according to the dynamic model of the system. In this regard, faster dynamic response are achieved but the computational burden is increased. Additionally and in comparison with modulator-based solutions, a more spread harmonic spectrum is seen with these strategies—note that the modulator allows the discrete control signal to switch within T_s, while this strategy fixes the output signal for the whole period T_s, and thus the spectrum is not expected to be concentrated.

Alternatively, and as a combination of the strategies above, there are some ones that explicitly model the modulator inside their formulation. To achieve this, instead of selecting the discrete control signal, they determine when every power device has to commute by means of the models of the system. The modulator formulation to obtain the same performance than (1.2) would be

$$\text{every } t \in [0,T_s] : \begin{cases} y & = y_0 \text{ for } \quad t < T_1 = u \in [0,T_s] \\ y & = \overline{y_0} \text{ for } \quad T_1 = u \leq t \leq T_s \end{cases} \tag{1.3}$$

where $y_0 = 0,1$ stands for the binary value of the output at the beginning of the period, and $\bar{y}_0$ for the opposite value. In this case, the control signal u is still continuous with range $u \in [0,T_s]$, the output remains discrete, while fast dynamics are achieved thanks to the knowledge of the model and the output spectrum is concentrated around the switching frequency and its multiples, similarly to those modulator-based strategies.

Despite the benefits of the strategies that do not require a modulator, the easiness of implementation and satisfactory results obtained when using modulator-based control strategies makes them the more widely accepted solution. Consequently, this work is more focused on modulation algorithms that use a modulation stage, although some additional

contributions that do not belong to that category are included.

Common control strategy

Most of the literature in power converter control are devoted to modulator-based solutions as they allow the use of continuous controllers, whose theory is well established in control engineering. In this regard, the commonly used control scheme is known as linear feedback controller, shown in Fig. 1.3, which implements a controller $C(s)$ whose input is the tracking error e and whose output is the input of the modulator d. The tracking error is computed from a reference var*, that is given externally, and the measured magnitude (var). The modulator input is the continuous control signal d and its output is the discrete gating signals y of the power devices of the converter. Note that the measuring and modulator stages take part in this closed-loop system and they have an impact in its dynamic performance. In digital systems, the measuring is achieved by means of an analog to digital converter (ADC) that samples the magnitude at a given sampling frequency F_{samp} [26] and holds it for the remaining of the period T_{samp}, which is modelled as a sample and hold (S&H) delay. Similarly, modulators receive a sampled value of d that is updated at the switching frequency f_s—which is equivalent to introducing a zero-order hold (ZOH) between d and the modulator input—, and the output is generated within its corresponding period T_s. Both cases introduce delays in the closed loop scheme, and some authors [27] model them as a single first-order transfer function with a gain K_{Mod} and a time constant $\tau = T_s/2 + T_{\text{samp}}$:

$$G_{\text{Mod+S\&H}}(s) = \frac{K_{\text{Mod}}}{1 + s\left(T_s/2 + T_{\text{samp}}\right)}, \tag{1.4}$$

where K_{Mod} is the scaling magnitude between the continuous control signal d and the averaged value of the discrete signal y. Nevertheless, in the control design process, it is usually assumed that the fundamental frequency of the variable under control (var) is low enough compared to the time constant of (1.4), and thus, the closed-loop performance is barely affected.

Modulation approaches

Focusing on fully controllable two-level grid-connected VSC converters, there are several methods that achieve proper modulation. The aim of the modulator is to resemble the continuous input signal, which is usually sinusoidal composed primarily of a fundamental component and, in some cases, some low-order harmonics. Thus it is desired that the frequency spectrum of the output matches these components.

PWM generates a quadratic pattern, i.e. a discrete signal $y = 0,1$, where the width of the square pulse is determined by the continuous input signal, i.e. the duty ratio $d \in [0,1]$. Recalling (1.2), by using large switching frequencies f_s in comparison with the frequencies that are desired to be modulated, the modulation objective can be properly achieved. As a result, the output spectrum matches the input one but for the addition of some components around the switching frequency (see Fig. 1.4) and its multiples. This is of great interest

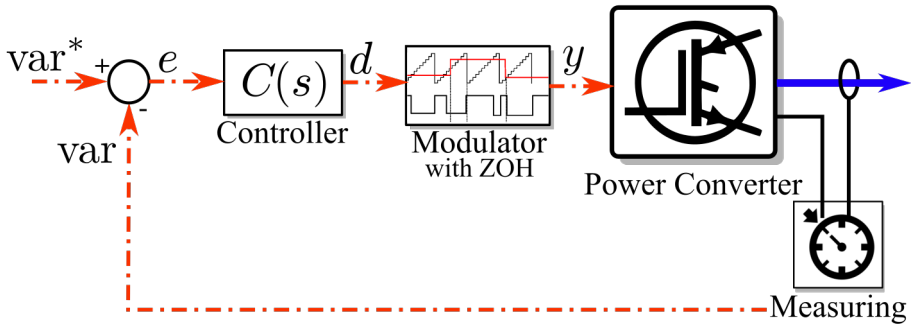

Figure 1.3 Scheme of a common linear feedback controller used for power converter control.

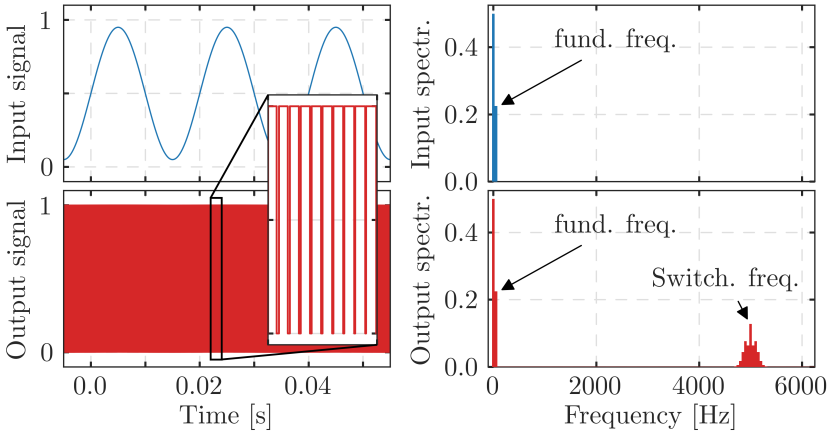

Figure 1.4 Example of a PWM generated with a pure sinusoidal signal of 50 Hz as input, with a switching frequency of 5000 Hz.

for VSC as the PWM pulses can represent at which point one phase is connected to the dc-link, that is, for a considered phase $i = a,b,c$

$$v_{iN} = \begin{cases} v_{dc}/2 & \text{if} \quad y = 1 \\ -v_{dc}/2 & \text{if} \quad y = 0 \end{cases}, \tag{1.5}$$

where v_{iN} is the voltage drop between phase i and dc-link neutral point N (see Fig 1.2). In this way, any continuous signal $v_i(t)$ whose range lies within $[-v_{dc}/2, v_{dc}/2]$ can be represented through this method. It is worth mentioning that there is a parameter called modulation index $m_i \in [0,1]$ for every phase i that represents the dc-link voltage utilization

as:

$$m_i = \max(v_i(t))/(v_{dc}/2) \tag{1.6}$$

where 'max' stands for the function that gives the maximum value over time. Then, having a modulation index larger than 1 means that the continuous signal is out of boundaries and the modulator will not be able resemble the input's spectrum. Nevertheless, many efforts have been put to extend the dc-link voltage utilization beyond unitary modulation index. A well-known solution for three-phase converters is the injection of a third-order harmonic [28] into the continuous signal, reducing the maximum value of the fundamental component, and taking advantage that third-order harmonic are neglected in the output spectrum of three-phase systems.

The methodology used to generate square pulses from the continuous signal is not unique. In this regard, two methodologies that uses PWM stands out in the literature: Carrier-based PWM and space-vector modulation (SVM) PWM.

Carrier-based PWM

This type of PWM uses carrier signals to generate the switching signals by means of simple comparison. The carrier is a periodic signal whose period matches the switching frequency one (T_s), and it is usually sawtooth or triangular shaped. The carrier also has the same practical bounds than the modulation's input. Then, if the result of the previous stage is outside these bounds the system is overmodulating.

For single-phase full-bridge systems (see Fig. 1.5a), which have 4 switching devices, there are two types of modulation: Bipolar and unipolar modulation. The difference in their implementation lies in whether they use one or two modulation signals to control the four devices. Note that two gating signals $\overline{S_1^a}$ and $\overline{S_1^b}$ are complementary to their counterpart S_1^a and S_1^b respectively. Therefore, the strategy followed by the bipolar modulation is to make $S_1^b = \overline{S_1^a}$ by using only one comparison. Consequently, the output v_{ab}—measured from point a to point b—is a square pulse that can be equal either to $-v_{dc}$ or v_{dc}, while the effective switching frequency is f_s. Alternatively, the unipolar modulation uses another modulation signal, which is equal to the input signal but 180°-shifted, to command S_1^b. Consequently, the square pulse can be equal either to $-v_{dc}$, 0 or v_{dc}, and thus the switching pulses are generated in such a way that the effective frequency of the output is doubled, while still keeping the same input-output harmonic resemblance than the bipolar modulation. With this approach, whenever the modulation signal is bigger than 0, $v_{ab}(t) = \{0, v_{dc}\}$, otherwise, $v_{ab}(t) = \{-v_{dc}, 0\}$.

A single-phase half-bridge AC-DC converter cannot use unipolar modulation as there is only one control signal. In these converters with only one phase arm, the AC negative side has to be connected to the dc-link mid-point (point N in Fig. 1.2), generating square pulses that go from $-v_{dc}/2$ to $v_{dc}/2$.

For three-phase two-level VSC (see Fig. 1.5b), a similar scheme of the bipolar modulation is implemented for each phase, but for the use of a three-phase set of modulating signals. Therefore, one common carrier is used while every phase has its own modulating signal, which are equal but 120º-shifted in balanced systems. In this way, the output voltage v_{in} of each phase, measured from point $i = a, b, c$ to the negative of the dc-link side

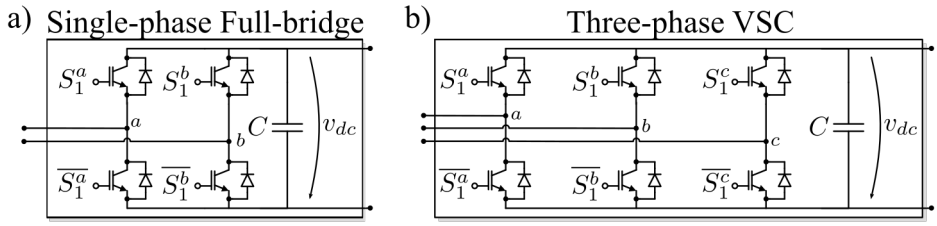

Figure 1.5 a) Single-phase full bridge AC-DC converter; b) Three-phase AC-DC VSC.

n, is a square wave that goes from 0 to v_{dc}. Due to this and that the modulating signals in three-phase systems are usually 120°-shifted between phases, the output voltages $v_{i_1 i_2}$, measured from phase $i_1 = a$,b,c to phase $i_2 = a$,b,c, goes from 0 to v_{dc} whenever the modulating signal of phase i_1 is bigger than the one of phase i_2, and goes from $-v_{dc}$ to 0 otherwise.

There exists other types of carrier-based modulations schemes for multilevel converters that use several carriers. These modulations will be presented later in the multilevel converter section.

Space vector modulation in three-phase VSC

Instead of considering three separated modulation signals (one per phase), a cartesian vector is used. In this regard, the original signals to be modulated (v_i for phase $i = a$,b,c) are represented as a three dimensional vector whose coordinates are known as abc coordinates. However, in a three-phase three-wire system, the common component can be neglected as its effect on AC magnitudes is suppressed, and thus a three-dimension to two-dimension transformation is used. The common transformation that isolates the common component is known as the Clarke transformation

$$T_{abc\to\alpha\beta} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \tag{1.7}$$

$$v_{\alpha\beta} = T_{abc\to\alpha\beta} v_{abc} \tag{1.8}$$

Thanks to this, a two-dimension vector in the so-called $\alpha\beta$ coordinates is obtained, which can be represented in a plane. With this, the common component lies perpendicular to this plane in the so-called γ component. Three-phase two-level VSC has 8 possible combinations of the switches—three binary signals {S_1^a, S_1^b, S_1^c} = 0,1 yields $2^3 = 8$ possibilities—and thus, 8 switching vectors represent the modulation region—referred as switching vectors S_1^a, S_1^b, S_1^c. Note that these combinations of switches can be positioned in a cube whose axes are abc as shown in Fig. 1.6. The $\alpha\beta$ transformation projects these axes in the $\alpha\beta$ plane in such a way that the common component (a=b=c) is no longer considered. In this way, any abc vector can be represented within this plane neglecting the common component. As a consequence, the switching vectors 000 and 111 appear in the same position, which exhibits that both positions have the same effect on the system performance.

Following with the modulation approach, the two-dimensional vector is located inside the modulation region in $\alpha\beta$, which turns out to be an hexagon, where all possible switching states are represented. Then, the easiest solution, is to consider the three closest switching states, which are weighted in such a way that the resultant linear combination matches the input vector. This procedure is carried out every switching time (T_s), and the selected switching states are sequenced according to this linear combination in such a way that the average value of the output voltage over T_s equals the input one.

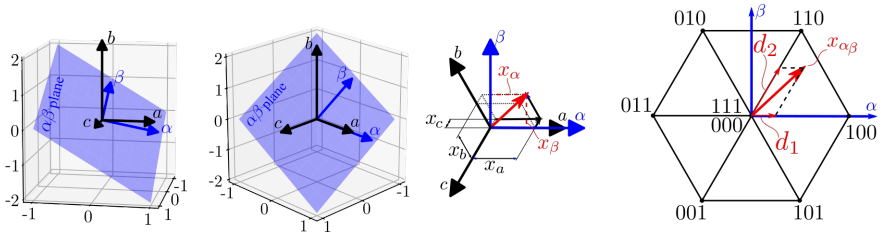

Figure 1.6 Three-dimensional representation of the $\alpha\beta$ transformation from abc coordinates, and corresponding space vector hexagon with one vector in the first sextant as example.

Figure 1.6 depicts the $\alpha\beta$ plane and its relation with the abc coordinates, along with the space vector hexagon. As an example, in Fig. 1.6, a vector $x_{\alpha\beta}$ is located inside the hexagon and the switching vectors (100), (110) and (000/111) are linearly combined to represent it. For this, the duty ratios of each switching vector—d_1 for vector (100), d_2 for vector (110), and d_3 for either vector (000) or (111)—must be computed such the following constraints are fulfilled:

$$x_{\alpha\beta} = \begin{bmatrix} d_1 & d_2 \end{bmatrix} \begin{bmatrix} T_{abc\to\alpha\beta}[100]^T \\ T_{abc\to\alpha\beta}[110]^T \end{bmatrix} \tag{1.9}$$

$$d_1 + d_2 + d_3 = 1, \tag{1.10}$$

where $x_{\alpha\beta}$ is the normalized vector of the desired output voltage transformed into the $\alpha\beta$ reference frame, i.e. $x_{\alpha\beta} := v_{\alpha\beta}/v_{dc}$ from (1.8)—note that the desired output voltage v_i is the output of the controller. This normalization comes from considering that signal $S_1^i = 1$ generates an output $v_{iN} = v_{dc}/2$, and $v_{iN} = -v_{dc}/2$ otherwise (see Fig. 1.2 and Eq. (1.5)). In this way, the output voltage vector can be normalized by dividing it by v_{dc}, so the duty ratio is directly related to this value. Equation (1.9) guarantees the proper vector modulation, and (1.10) comes from the definition of duty ratio. With this procedure, any vector that lies inside the hexagon can be represented while fulfilling the previous constraints.

There is an inherent degree of freedom in this procedure once the switching vectors are selected and its corresponding duty ratios are computed, that is the time-sequencing of such vectors. Usually they are sequenced in time following a clockwise or counter-clockwise scheme in the $\alpha\beta$ plane, but some applications present different approaches to achieve additional objectives [29, 30].

This scheme of SVM can be further extended for converters with more switching states following the same principle. For those cases, the hexagon should include more regions and switching states such that all feasible switching combinations are covered. Additionally, given the increased complexity of these extended converters, the vector selection is not restricted to the three-nearest ones, but any linear combination can be considered as long as the output voltage vector is properly modulated and the sum of all corresponding duty ratios is equal to 1.

Optimal PWM schemes

There is also a modulator category called optimal PWM schemes, where the switching pattern is computed beforehand using a set of trigonometrical equations. These techniques decide the number of commutations m considered per period, that is the number of instants where the switching devices must commute, and solves a system with m equations such those instants are determined. These strategies are commonly used for high-power applications where low number of commutations are desired due to the large switching losses they may have. In this regard, the larger the m, the more control over the output voltage harmonic spectrum. The most common modulation is the selective harmonic elimination PWM (SHE-PWM), where the switching instants (referred as switching angle over the grid period α_m) are computed such that the main component has a desired amplitude, and $m-1$ harmonics are removed. Alternatively, other objectives can be sought, such as grid compliance with the selective harmonic minimization (SHM-PWM) method, or overall reduction of the total harmonic distortion with optimal pulse patterns (OPP-PWM). They all use the Fourier decomposition of the periodical waveform to set the system of equations, while the α_m variables are obtained through numerical methods—for low values of m—or optimization algorithms such as linear programming or particle swarm optimization—for larger values of m.

1.2.4 Typical controllers for grid-connected power converters

This subsection is devoted to present some of the most typical controllers used for power converters—being most of them linear—, their usual control objectives and how they are implemented. As it was stated previously, it is necessary to use a modulator for these approaches as an interface between the continuous output of the controller and the discrete switching input signals of the power converter. As it is shown in Fig. 1.3, it is common to implement a linear feedback controller scheme [31], where a system variable reference var^* is tracked. For this, the controller inputs the tracking error e and outputs the desired average value of the system output—usually expressed as a normalized value that is related to the duty ratio d. This value is later introduced into the modulator to generate the switching pulses of the system. However, there exists some sources of error represented as disturbances in Fig. 1.7a). In this regard, the disturbances are shown as, on the one hand, $\widetilde{\text{var}}$ to represent possible noise that can appear during the measuring process, and, on the other hand, $\tilde{y}$ to represent the modifications caused by the hardware and software implementations (quantization errors, delays, hardware constrains, etc.). To analyze such effects from the control perspective, Fig. 1.7b) is shown, where the system is replaced by its model $G(s)$ and the different input-output relationship can be obtained.

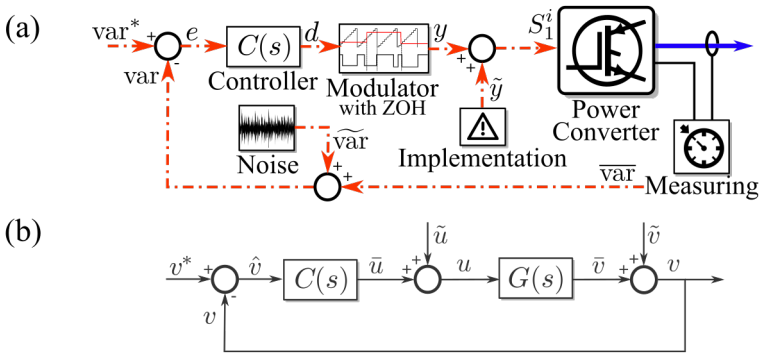

Figure 1.7 Scheme of the common linear feedback controller with the sources of error represented as external disturbances. (a) Scheme with modulator, power converter, measuring and sources of disturbances; (b) Generic scheme using the system model $G(s)$.

In this figure, the measured system variable to regulate is v, whose reference value is v^*, and tracking error $\hat{v}$; the control input is $\bar{u}$; the control signal that inputs the system is u, and the system output variable is $\bar{v}$. The disturbances generated in the control and modulation stages, such as those related to the implementation procedure, are denoted as $\tilde{u}$; whereas the disturbances generated in the measuring process or due to modelling errors are denoted as $\tilde{v}$. Consequently, the following transfer functions can be obtained:

$$v(s) = T(s)v^*(s) + D_u(s)\tilde{u}(s) + D_v(s)\tilde{v}(s), \tag{1.11}$$

where $T(s)$ is the tracking transfer function, $D_u(s)$ is the transfer function for disturbances in u, and $D_v(s)$ is the transfer function for disturbances in v. Considering the closed-loop of Fig. 1.7, the transfer functions can be expressed in terms of the controller $C(s)$ and the system model $G(s)$ as:

$$T(s) = \frac{C(s)G(s)}{1 + C(s)G(s)} \tag{1.12}$$

$$D_u(s) = \frac{G(s)}{1 + C(s)G(s)} \tag{1.13}$$

$$D_v(s) = \frac{1}{1 + C(s)G(s)}. \tag{1.14}$$

These equations exhibit that the controller design determines not only the tracking response, but also the disturbance rejection. For those cases where a modulator is being used, it is worth mentioning that the controller bandwidth is usually much lower than the switching frequency (f_s) of the system. The reason is twofold: the modulator introduces additional components in the output spectrum around the switching frequency or its multiples, which could affect the response in the closed-loop dynamic if any of these components lies

within the controller bandwidth; and indirectly due to the fact that digital systems usually synchronize the system execution and sampling with the switching frequency of the PWM, therefore it is desired to have relatively high values of f_s.

In the following, the most seen linear controllers used in the literature will be presented: the proportional-integral (PI) controller and the proportional-resonant (PR) controller.

PI Controller

It is one of the most used controllers in control engineering due to its simplicity and good performance. Its continuous and frequency domain well-known expressions are:

$$y(t) = K_p u(t) + K_i \int_0^t u(\tau) d\tau \ , \quad C_{\text{PI}}(s) = K_p + \frac{K_i}{s}, \tag{1.15}$$

which is the addition of a proportional part of the input and its computed integral over time. Terms K_p and K_i are the controller parameters whose tuning is explained more in detail in subsection 1.2.4. This controller response is well suited for DC or constant magnitudes due to its high gain at low frequencies, while having the proportional gain to handle the transitory. The Bode diagrams of such controller for $K_p = 1$ and $K_i = 1$,10,100 are shown in Fig. 1.8. Nevertheless, the limited response of this controller to AC magnitudes, which are very common in grid-connected systems, requires to translate the controller signals from sinusoidal to constant values. For this, the system variables are expressed in the dq reference frame—which stands for direct-quadrature—also called synchronous reference frame. This reference frame rotates at the same frequency than the considered AC magnitude, and thus the magnitude expressed in these axes appears as a DC component. Then, the controller output can be translated back to the stationary reference frame. By including this change of reference frame, the PI controller can be used to compensate certain AC magnitudes. The dq vector is obtained as follows

$$x_{dq} = T_{abc\to dq}\, x_{abc} \ , \quad T_{abc\to dq} = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{pmatrix}, \tag{1.16}$$

where θ is the rotation angle of the AC magnitude.

As it was mentioned in the SVM for three-phase VSC section, it is common to express the three-phase magnitudes in $\alpha\beta$ following the transformation given in (1.7). Considering that the $\alpha\beta$ components are orthogonal, its transformation to the dq reference frame can be performed by just using the rotation matrix $L_{\text{rot}}(\theta)$:

$$x_{dq} = L_{\text{rot}}(\theta) x_{\alpha\beta} \ , \quad L_{\text{rot}}(\theta) = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}, \tag{1.17}$$

where x_{dq} is the two-component vector expressed in the synchronous reference frame, and θ is the angle of the AC magnitude that synchronizes the dq axes.

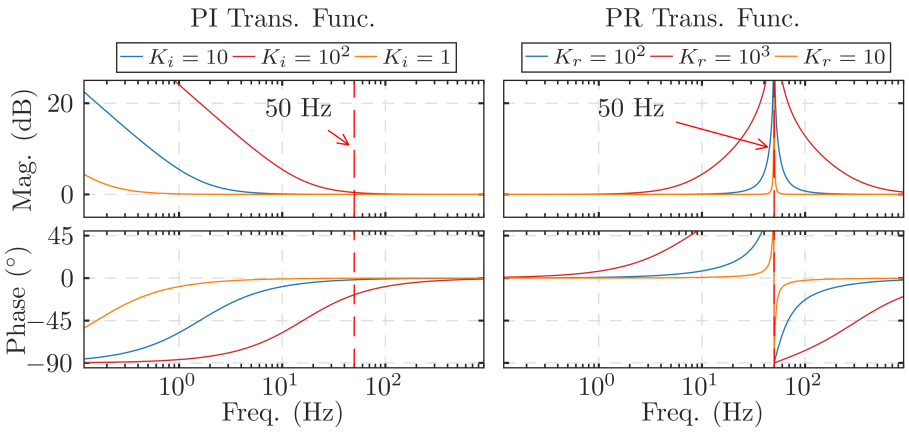

Figure 1.8 (Left) Bode plot of PI Controller with $K_p = 1$ for different values of $K_i =$ 10,100,1. (Right) Bode plot of ideal PR Controller with $K_p = 1$ for different values of $K_r = 10^2$,10^3,10.

In any case, the obtainment of such an angle can be performed by means of the application of a phase-locked loop to the grid voltage measurements. The following paragraph describes its most basic implementation.

Phase-locked loop (PLL)

To obtain the value of $\theta = \omega_g t$ used in (1.16) and (1.17) a phase-locked loop (PLL) scheme is used, which basically tracks the phase angle of the voltage measurements. The basic scheme usually comprises a phase detector (PhDet), a low pass filter (LPF) and a voltage controlled oscillator (VCO) [32]. The phase detector measures the phase difference between the PLL input and output, the low-pass frequency rejects the high-frequency components of this difference, and the VCO generates the output signal based on the filtered difference. The most basic configuration of synchronous reference frame PLL uses the $T_{abc\to dq}$ transformation that outputs the q component as the PhDet, a PI filter as the LPF, and an integrator as the VCO which outputs the grid angle θ that feedbacks the PhDet. This scheme is shown in Fig. 1.9.

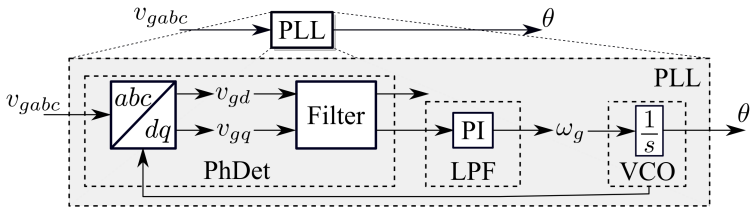

Figure 1.9 Basic scheme of a PLL for grid synchronization.

Resonant controller

Considering the problematic given by the PI controller for AC magnitudes, an alternative to use the PI and the dq reference frame is to modify the integral action of the PI controller in such a way that it acts as a resonator for a specific frequency ω_r. With this, infinite gain in the controller response at ω_r is achieved. This stage is known as resonant controller and, together with the proportional part, it has the following transfer function :

$$C^{\text{PR}}(s) = K_p + \frac{K_r s}{s^2 + \omega_r^2}, \tag{1.18}$$

where K_r and ω_r are the new control parameters for the resonant part. This controller expression comes from the expression of a PI controller in synchronous reference frame translated to the stationary one. For this, the following expression shows the relation when transforming from one reference frame rotating at ω to the stationary one

$$C(s)_{\text{Sync.}} = \frac{1}{2}\left(C(s + j\omega) + C(s - j\omega)\right). \tag{1.19}$$

where the frequency is shifted $\pm j\omega$ in the s domain. Indeed, a proportional-resonant controller tuned at ω in stationary frame is equivalent of two proportional-integral controllers each one in a synchronous reference frame rotating at ω and $-\omega$ respectively [33]

$$\begin{aligned}\left(K_p + \frac{K_i}{s}\right)_{\text{Sync.}} &= \frac{1}{2}\left(K_p + \frac{K_i}{s + j\omega} + K_p + \frac{K_i}{s - j\omega}\right) \\ &= \frac{1}{2}\left(2K_p + \frac{2K_i s}{s^2 + \omega^2}\right)\end{aligned} \tag{1.20}$$

However, infinite gain for AC magnitudes could yield instability issues in the closed-loop scheme. Besides, any possible mismatch between the grid fundamental frequency with the established ω_r could make the resonant part to not properly track the AC component. For this, the non-ideal PR is used instead, where a non-ideal integrator—previous to be shifted in frequency—is used: $1/s \rightarrow 1/(1 + s/\omega_c)$ [34]. Therefore, when this integrator is shifted a frequency ω_r and combined with the proportional part, the following transfer function for the non-ideal PR controller is obtained:

$$C^{\text{PR}_{\text{non-ideal}}} = K_p + \frac{K_r \omega_c s}{s^2 + 2\omega_c s + \omega_r^2}, \tag{1.21}$$

where ω_c is the cut-off frequency of the low-pass filter used for the non-ideal integrator, that is chosen to be $\omega_c \ll \omega_r$. As a result, the bandwidth of the resonant part is widened,—the larger the value of ω_c, the wider the bandwidth—in spite of its magnitude response being more limited, but it is large enough to track the AC magnitude properly.

Frequency-locked loop (FLL)

In a similar way that the grid angle θ is required for the synchronous reference frame, the PR controller in stationary frame requires the knowledge of the grid frequency ω_g. This can

be achieved by means of a frequency-locked loop (FLL) which extracts the grid frequency from the grid voltage measurements. There are several FLL schemes. However, the FLL based on the second-order generalized integrator (SOGI) is one of the most accepted ones as it can be used in single-phase systems [35]. The SOGI performs as a band-pass filter with K as its gain and two outputs: one output (v'_g) has zero dB magnitude and no phase-shift for a specific resonant frequency, whereas the second one (qv'_g) achieves the same attenuation for the same frequency component but delayed 90°—which is referred as the quadrature output. Consequently, using the measured grid voltage $v_{g\alpha}$ as input, its filtered component at ω_g and its 90°-shifted version $v'_{g\beta}$ are obtained. The FLL scheme is integrated along the SOGI diagram as shown in Fig. 1.10, where a simple auto-tune block with gain γ is implemented to obtain the resonant frequency of the SOGI-QSG, which matches the grid frequency one (ω_g).

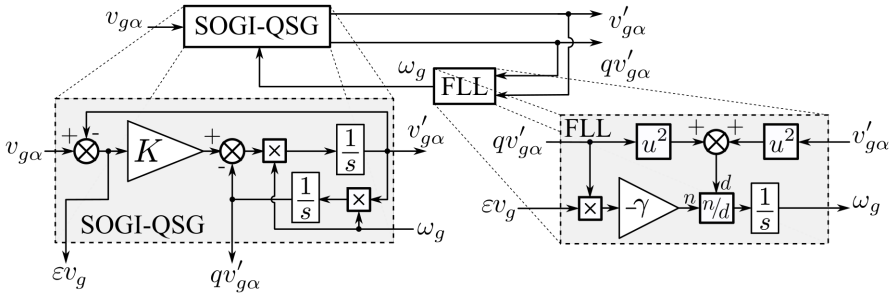

Figure 1.10 Basic scheme of a SOGI-QSG-based FLL for grid frequency obtention.

Cascaded configuration

This subsection is devoted to present one of the most typical control schemes of three-phase grid-connected VSC. This scheme is the cascaded-control loop shown in Fig. 1.11 where an outer control (OC) loop outputs the references for the inner control (IC) loop [36]. The principle that allows this is the difference between the dynamic responses, as the outer loop control bandwidth is much smaller than the inner loop control one, and thus it allows both controller to track their respective references without interfering in each other's response.

As shown in Fig. 1.11, the outer control loop computes the current references—whether in $\alpha\beta$ or in dq reference frame—for the inner control loop, which implements a current controller to track them. The outer control loop can be designed to track the active and reactive power p and q, given their respective references (p^*,q^*) (Block 1). Alternatively, the active power reference p^* can be regulated using a PI controller to make v_{dc} to track its reference v^*_{dc} (Block 2). In the latter case, the current references can be computed from p^* and q^* by using the instantaneous power theory (IPT) [37]:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ -v_{g\beta} & v_{g\alpha} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \rightarrow \begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix} = \frac{1}{v^2_{g\alpha} + v^2_{g\beta}} \begin{bmatrix} v_{g\alpha} & -v_{g\beta} \\ v_{g\beta} & v_{g\alpha} \end{bmatrix} \begin{bmatrix} p^* \\ q^* \end{bmatrix}. \tag{1.22}$$

where the instantaneous active and reactive power and their references are denoted as p,q,p^*,q^*, respectively. The current references inputs the inner control loop that is carried out either in synchronous reference frame such that $i_{dq} \rightarrow i^*_{dq}$ (Block 3) or in stationary reference frame $i_{\alpha\beta} \rightarrow i^*_{\alpha\beta}$ (Block 4). In the first case, a PI controller is used together with a decoupling term $w_g L$ as it will be explained later. In the second case, the PR controller is used as long as the resonant frequency is tuned at the grid-frequency ω_g. In any case, the outputs are transformed back to the abc reference frame and a feedforward term of the grid voltages v_{gabc} is added (Block 5) as it will be explained later. Note that the reference frame transformation step inherits one degree of freedom, that is the one associated to the homopolar component, as it involves an $\mathbb{R}^2$ to $\mathbb{R}^3$ transformation. The resulting variables v_{abc} are the desired output voltages to modulate, which are normalized using the dc-link voltage v_{dc} and are input into the modulator such that the switching signals S_1^a, S_1^b, S_1^c are generated.

It is common to use the outer control loop to compute the current references in such a way that the the dc-link voltage and the reactive power reference are properly tracked, i.e. $v_{dc} \rightarrow v^*_{dc}$ and $q \rightarrow q^*$. In the following, the dc-link voltage and AC current models along their typical controllers are exposed.

dc-link voltage controller

As it is shown in Fig. 1.11, one way to compute the active power reference p^* is by regulating the dc-link voltage towards its reference. This is the case for AC/DC or DC/AC converters that use a capacitor as the DC storing element in the converter, whose voltage can be regulated adjusting the active power flow. In this regard, any mismatch in the subtracted AC and DC active power would necessarily affect the dc-link voltage value. For example, when the power flow that inputs the converter from the AC side is larger than the one subtracted from the DC side, the dc-link voltage increases. Therefore, the dc-link voltage steady-state condition is reached when the AC and DC power flows match. In order to model the dc-link voltage, it is assumed that the power converter has no losses and it has ideal devices. Therefore the instantaneous capacitor voltage equation results in

$$C\frac{dv_{dc}(t)}{dt} = i_{dc}(t) = i_a S_1^a + i_b S_1^b + i_c S_1^c,$$

which can be averaged over a switching period T_s using the duty ratio definition $d_i = 1/T_s \int_{t_k}^{t_k+T_s} S_1^i d\tau$ as

$$C\frac{dv_{dc}}{dt}|_{T_s} = i_a d_a + i_b d_b + i_c d_c.$$

Considering that the stored DC energy is equal to $Cv_{dc}^2/2$, the dynamic can be derived in terms of power as

$$\frac{d}{dt}\left(C\frac{v_{dc}^2}{2}\right) = v_{dc}C\frac{dv_{dc}}{dt} = v_{dc}(i_a d_a + i_b d_b + i_c d_c) = i_a v_a + i_b v_b + i_c v_c = p, \tag{1.23}$$

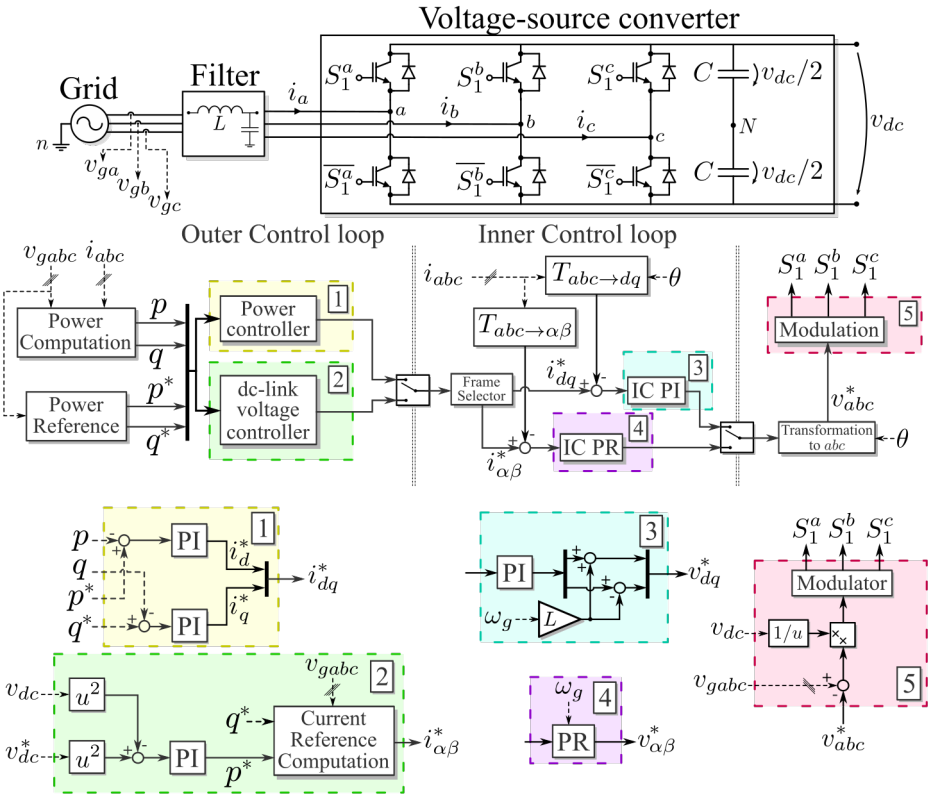

Figure 1.11 Scheme of the typical cascaded control loop used for grid-connected VSC with CCs at both reference frames, two options for power objectives, and modulation stage. 1: Outer control loop based on external active and reactive power reference. 2: Outer control loop based on external reactive power reference and dc-link voltage regulation. 3: Inner control loop in synchronous reference frame based on PI controller. 4: Inner control loop in stationary reference frame based on PR controller. 5: Grid voltage feedforward term.

where $v_i = d_i v_{dc}$ was recalled from the normalization step, and the instantaneous active power theory is applied [37]. In this way, the transfer function is given as:

$$G_{dc}(s) = \frac{v_{dc}(s)}{p(s)} = \frac{1}{V_{dc} C s}, \tag{1.24}$$

where v_{dc} can be approximated by the value of V_{dc} at the desired operating point. Consequently, if it is assumed that the inner control loop would make $p \to p^*$, variable v_{dc}^2 would be regulated towards ${v_{dc}^*}^2$ by means of a PI controller whose output is p^*. At the same time, variable q^* can be set externally to fulfill other control objectives without affecting the dc-link voltage.

The open-loop expression of the outer loop is then given as:

$$G_{\mathrm{OC_{ol}}}(s) = C_{\mathrm{PI}}(s) G_{\mathrm{IC_{cl}}}(s) G_{dc}(s) = \frac{(K_p s + K_i) G_{\mathrm{IC_{cl}}}(s)}{s^2 V_{dc} C}, \tag{1.25}$$

where $C_{\mathrm{PI}}(s)$ is the PI controller transfer function, and $G_{\mathrm{IC_{cl}}}(s)$ is the transfer function of the closed-loop inner controller that will be derived in the following subsection.

AC current controller

The inner control loop is usually a current controller that determines the required output of the converter to make $i_i \to i_i^*$ for $i = a,b,c$, which is equivalent to make $p \to p^*$ and $q \to q^*$ if the references are properly computed (1.22). As it is shown in Fig. 1.11, the current references are given externally to the inner control loop so the current controller has to be designed taking into account the dynamic model of the three-phase currents. Considering the Kirchhoff's law in the scheme of Fig. 1.11, the dynamical equations of the currents are:

$$L\frac{di_i}{dt} + R_L i_i = v_{gi} - v_i\,, \quad i = a,b,c\,, \tag{1.26}$$

where an one-stage L-filter with parasitic resistance R_L is considered, variable v_{gi} refers to the grid voltage of phase i, and v_i is the phase i of the converter output. However, the current controllers are applied either in stationary reference frame $\alpha\beta$ or synchronous reference frame dq, therefore Eq. (1.26) should be transformed first:

$$\text{Stationary reference frame: } L\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + R_L \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} v_{g\alpha} \\ v_{g\beta} \end{bmatrix} - \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{1.27}$$

$$\text{Synchronous reference frame: } L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + R_L \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} - \begin{bmatrix} v_d \\ v_q \end{bmatrix} + \underbrace{\omega_g L \begin{bmatrix} -i_q \\ i_d \end{bmatrix}}_{\text{dec. term}}. \tag{1.28}$$

The decoupling term that appears in Eq. (1.28) comes from the derivative of the rotation matrix $L_{\mathrm{rot}}(\omega_g t)$ when it is applied to the stationary reference frame:

$$\begin{aligned} \frac{d}{dt}\left(L_{\mathrm{rot}}(\omega_g t) \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \right) &= \omega_g \begin{bmatrix} -\sin(\omega_g t) & \cos(\omega_g t) \\ -\cos(\omega_g t) & -\sin(\omega_g t) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + L_{\mathrm{rot}}(\omega_g t) \frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \\ &= \omega_g \begin{bmatrix} i_q \\ -i_d \end{bmatrix} + \frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix}. \end{aligned}$$

Therefore, the controller output $v_{\alpha\beta}^*$ or v_{dq}^* can be defined inspired from both dynamical equations (1.27)–(1.28) by adding the grid voltages as feedforward terms and the decoupling term :

$$\begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} := -\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} + \begin{bmatrix} v_{g\alpha} \\ v_{g\beta} \end{bmatrix}$$

$$\begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} := -\begin{bmatrix} v_d \\ v_q \end{bmatrix} + \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} + \omega_g L \begin{bmatrix} -i_q \\ i_d \end{bmatrix},$$

which inserted into (1.27)–(1.28) results in the following dynamical equations:

$$\text{Stationary reference frame: } L\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + R_L \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \tag{1.29}$$

$$\text{Synchronous reference frame: } L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + R_L \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix}. \tag{1.30}$$

Then, the transfer function $G_{\text{c}}(s)$ that defines the current response can be obtained for each reference frame and axis as:

$$\text{Stationary reference frame: } G_{\text{c}}(s) = \frac{i_{\alpha\beta}(s)}{v^*_{\alpha\beta}(s)} = \frac{1}{R_L + Ls} \tag{1.31}$$

$$\text{Synchronous reference frame: } G_{\text{c}}(s) = \frac{i_{dq}(s)}{v^*_{dq}(s)} = \frac{1}{R_L + Ls}, \tag{1.32}$$

where $i_{\alpha\beta}$ and i_{dq} are the current vectors. Despite the fact that the transfer functions are equal, the current control loop inputs in the stationary reference frame are AC, whereas in the synchronous reference frame are DC magnitudes. It is also worth mentioning that, thanks to the feedforward and decoupling terms, both axis inside each reference frame share the same dynamics and they are uncoupled—Eq. (1.31)–(1.32) define two transfer functions each—, and thus they can be analyzed and controlled individually following the same principle. Considering this, one axis closed-loop behaviour will be studied for control design.

For the inner control loop, and in contrast to the outer loop, the use of the modulator may affect the closed-loop dynamic, and thus it should be included in the closed-loop analysis. To this end, it is assumed that the modulator stage takes some time to implement the desired output voltage v_i, and thus it is represented by a first-order approximation of a delay $G_d(s)$. In this way, the open-loop inner current control results in:

$$\begin{aligned} G_d(s) &= \frac{1}{1+1.5T_s s}, \\ G_{\text{IC}_{\text{ol}}}(s) &= C_{\text{C}}(s)G_d(s)G_{\text{c}}(s) = C_{\text{C}}(s)\frac{1}{(1+1.5T_s s)}\frac{1}{(R+Ls)} = \\ &= C_{\text{C}}(s)\frac{1}{(1+1.5T_s s)}\frac{T_c}{L(1+T_c s)}, \quad T_c = \frac{L}{R} \end{aligned} \tag{1.33}$$

where $C_{\text{C}}(s)$ is the controller transfer function, T_c is the L-filter time constant, and $G_d(s)$ considers a delay of 1.5 times the sampling time (T_s) [27], which corresponds to the measuring S&H and modulator implementation delays. Therefore, the closed-loop for the inner control can be modelled as

$$G_{\text{IC}_{\text{cl}}}(s) = \frac{C_{\text{C}}(s)T_c}{L(1+1.5T_s s)(1+T_c s)+C_{\text{C}}(s)T_c} \tag{1.34}$$

At this point, the expected response of the closed-loop varies depending on the considered reference frame.

For the case of the stationary reference frame, where the current references $i^*_{\alpha\beta}$ are sinusoidal, it is expected to have some controllability degree around the AC frequency, which is achieved by means of a resonant controller. Indeed, the high gain of the resonant part at the considered AC frequency guarantees proper tracking of the reference. As an example, the frequency response of the transfer function of the closed-loop inner control (1.34), with $C^{\text{PR}_{\text{non-ideal}}}$ (1.21) instead of $C_{\text{C}}(s)$, is depicted in Fig. 1.12. Note that the PR controller ideally tuned ($K_r = K_r^*$), whose tuning process will be explained later, achieves tracking of the reference around ω_g given that it has 0 dB and no phase-shift. Moreover, to depict the effect of a badly tuned controller, the transfer function with K_r 100 times larger and smaller than K_r^* are also plotted.

Alternatively, when using synchronous reference frame, the inputs are DC magnitudes so a PI controller is a valid candidate to track such magnitudes. By replacing $C_{\text{C}}(s)$ for $C_{\text{PI}}(s)$ (1.15), the following $G_{\text{IC}_{\text{cl}}}(s)$ is obtained:

$$G_{\text{IC}_{\text{cl}}}(s) = \frac{(K_p s + K_i)T_c}{Ls(1+1.5T_s s)(1+T_c s)+(K_p s+K_i)T_c}, \tag{1.35}$$

which can be further simplified in the analysis by tuning the integral gain as $K_i = \frac{K_p}{T_c}$ such that the integrator time constant matches the system one T_c, which results in:

$$G_{\text{IC}_{\text{cl}}}(s) = \frac{K_p}{Ls(1+1.5T_s s)+K_p}. \tag{1.36}$$

Notice that (1.36) is a second-order system whose analysis would yield some tuning criteria as it will be shown in the next subsection. Similarly to the PR controller, the closed-loop response of the inner controller when using a PI controller is depicted in Fig. 1.12, for an ideally tuned controller $K_i = K_i^*$, and two not properly tuned ones $K_i = K_i^*/100, K_i^* \cdot 100$. As it can be seen, the Bode plot is equal to that of a second-order system that can handle DC magnitudes with 0 dB and no phase-shift. However, notice that, for $K_i = K_i^*/100$, there is a slight peak in the magnitude close to the natural frequency, which, for a second-order system, means that an undesired overshoot is expected in the step response of the system.

Summarizing all the above mentioned, Fig. 1.13 depicts the simplified model in abc of the cascaded control where the two linear feedback control loops are used: the OC that computes the power reference p^* through a PI controller, and the IC that uses a current controller $C_c(s)$ to regulate the currents. This scheme can be extended to $\alpha\beta$ and dq. However, the effects the PLL or FLL may have on the IC performance can be

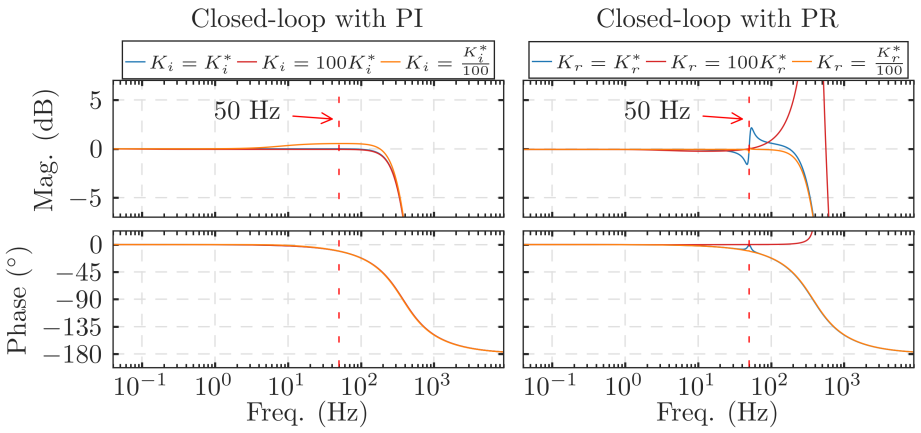

Figure 1.12 Bode diagram of the closed-loop inner control transfer function (1.34) when a PI and a PR controller is used. Variable K_i^* and K_r^* refers to the integral and resonant ideal control parameters, whose tuning is exhibited below. K_p is the same for both parameters and equal to K_p^*. System parameters are $R = 0.01\,\Omega$, and $L = 2\,m$H.

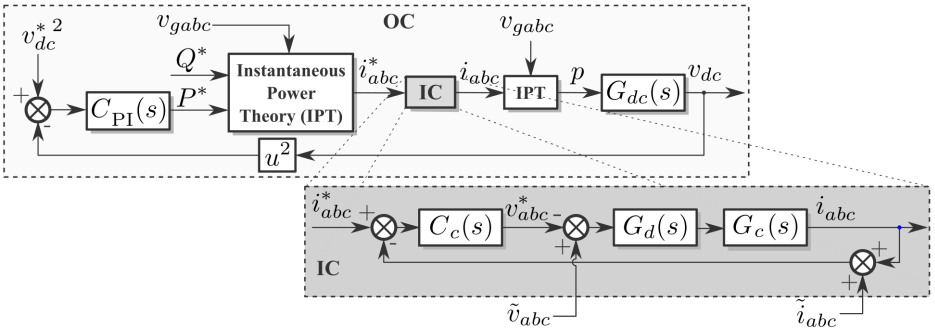

Figure 1.13 Simplified model of the cascaded configuration with two linear feedback control loops. Signals $\tilde{v}_{abc}$ and $\tilde{i}_{abc}$ represents the digital and control disturbances and the analog disturbances, respectively.

modelled through external input $\tilde{v}_{abc}(s)$ that acts as digital and control perturbations. Besides, input $\tilde{i}_{abc}$ acts as the analog disturbance, i.e. measurement noises in the grid currents.

Alternatives to PI or PR Controllers for the inner control loop

Instead of designing a controller to regulate the AC currents, the instantaneous powers can be aimed instead [38]. In it, a model-based term $y_{\alpha\beta}^{\mathrm{eq}}$ that would set $\frac{dp}{dt} = 0$ and $\frac{dq}{dt} = 0$ is computed, whereas incremental variables make the instantaneous active and reactive power tracking error go to zero. The vector expression for this controller is the following

$$v_{\alpha\beta} = v_{\alpha\beta}^{\text{eq}} + K_p(p-p^*)v_{g\alpha\beta} + K_p(q-q^*)Jv_{g\alpha\beta} \tag{1.37}$$

$$v_{\alpha\beta}^{\text{eq}} = \frac{2}{v_{dc}}\left(1+\frac{\tilde{X}q}{|v_{g\alpha\beta}|^2}\right)v_{g\alpha\beta} - \frac{2}{v_{dc}}\left(\frac{\tilde{X}p}{|v_{g\alpha\beta}|^2}\right)Jv_{g\alpha\beta} \tag{1.38}$$

$$\tilde{X} = -\gamma q p^*; \quad J = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$$

where γ is a positive constant that acts as an adaptation gain—to compensate for model errors—, $v_{\alpha\beta}$ is the already normalized output of the controller that also includes the feedforward term of the voltage grids, q and p are the instantaneous reactive and active powers, q^* and p^* are their respective references, and J is the 90°-degree rotation matrix.

Another current controller that works on stationary reference frame is the so-called hybrid repetitive controller [39]. It consists of a proportional gain in parallel to a repetitive scheme, which inputs the current error and a negative feedback plus a negative feedforward terms. These terms comes from a single delay of half the fundamental period. As a result, the equivalent transfer function is that of a PR plus infinite resonant terms tuned for the odds harmonic of the fundamental frequency. In this way, the controller is able to compensate for all odd harmonics. The transfer function of this controller $R(s)$ is initially expressed and later derived as

$$R(s) = \frac{1-e^{-\frac{s\pi}{\omega}}}{1+e^{-\frac{s\pi}{\omega}}} = \frac{e^{\frac{s\pi}{2\omega}}-e^{-\frac{s\pi}{2\omega}}}{e^{\frac{s\pi}{2\omega}}+e^{-\frac{s\pi}{2\omega}}} = \tanh\left(\frac{s\pi}{2\omega}\right) = \frac{2\omega}{\pi}\sum_{n=1}^{\infty}\frac{2s}{s^2+(2n-1)^2\omega^2}, \tag{1.39}$$

where it can be seen that the first term expresses the negative feedback and forward terms. The work [39] also proposes some practical modifications to damp the infinite gain similarly to the non-ideal PR controller, along with a simple low-pass filter to limit the controller bandwidth.

Tuning of common controllers and digital implementation

The PI and PR controllers are suitable for any grid-connected application, however the response entirely depends on the control parameters. For this, the tuning of such parameters is critical. In the following, some usual procedures for tuning these controllers are shown, however, other criteria might be used.

AC current controller

Considering the inner loop with the PI controller where the integral gain K_i has already being assigned to compensate for the system dynamic, the second-order system shown in (1.36) is used. Accordingly,

$$G_{\text{IC}_{\text{cl}}} = \frac{K_p}{Ls(1+1.5T_s s)+K_p} = \frac{\frac{2K_p}{3T_s L}}{s^2+\frac{2}{3T_s}s+\frac{2K_p}{3T_s L}}, \tag{1.40}$$

where the natural frequency ω_n and damping ratio ζ can be obtained as:

$$\omega_n = \sqrt{\frac{2K_p}{3T_s L}}; \quad \zeta = \frac{\sqrt{L}}{\sqrt{6K_p T_s}}. \tag{1.41}$$

An interesting procedure for second-order system is to make $\zeta = 1/\sqrt{2}$—fastest response while limited overshoot of 5% against an input step [40]. Therefore,

$$K_p = \frac{L}{3T_s}; \quad K_i = \frac{K_p}{T_c} = \frac{L}{3T_s T_c} = \frac{R}{3T_s}. \tag{1.42}$$

With the IC being tuned, a common assumption that is carried out in order to simplify the frequency analysis of the outer control loop is to simplify the IC closed-loop transfer function as a first-order system [3]:

$$G_{\text{IC}_{\text{cl}}} \approx \frac{1}{1+3T_s s},$$

where the time constant of the closed-loop system is estimated as $3T_s$, and thus the IC bandwidth is approximated by $f_{\text{bw}}^{\text{ICC}} = 1/(6\pi T_s)$. For this, the inner control loop has to be properly tuned as explained above.

For the case of the PR controller, the tuning process should aim to make the open-loop bandwidth—approximated with the crossover frequency, i.e the frequency that gives 0 dB in magnitude—much smaller than the system one [1/10,1/20] while also achieving a desired phase margin PM_{bw}^* for that frequency. Firstly, K_p can be derived from (1.33) assuming that the resonant part has no impact in the magnitude response nor in the phase around the IC bandwidth,

$$G_{\text{IC}_{\text{ol}}}(j\omega_{\text{bw}}) = K_p \frac{T_c}{L(1+1.5T_s j\omega_{\text{bw}})(1+T_c j\omega_{\text{bw}})} \tag{1.43}$$

where ω_{bw} is the bandwidth frequency in rad/s. With this and some approximations, the value of ω_{bw} can be selected in such a way that it fulfills the desired phase margin. Thus,

$$\begin{aligned} \angle G_{\text{IC}_{\text{ol}}}(j\omega_{\text{bw}}) &= \pi - \text{PM}_{\text{bw}}^* \frac{2\pi}{360^\circ} \\ 1.5T_s\omega_{\text{bw}} &= -\frac{\pi}{2} + \pi - \text{PM}_{\text{bw}}^* \frac{2\pi}{360^\circ} \\ \omega_{\text{bw}} &= \left(\frac{\pi}{3} - \text{PM}_{\text{bw}}^* \frac{\pi}{270}\right) f_s. \end{aligned} \tag{1.44}$$

Afterwards, the value of K_p can be obtained to make ω_{bw} the actual bandwidth frequency—again, roughly approximated by the crossover frequency—, that is making $|G_{\text{IC}_{\text{ol}}}(j\omega_{\text{bw}})| = 0$ dB,

$$K_p = \omega_{\text{bw}} L \sqrt{(1.5T_s\omega_{\text{bw}})^2 + 1} \tag{1.45}$$

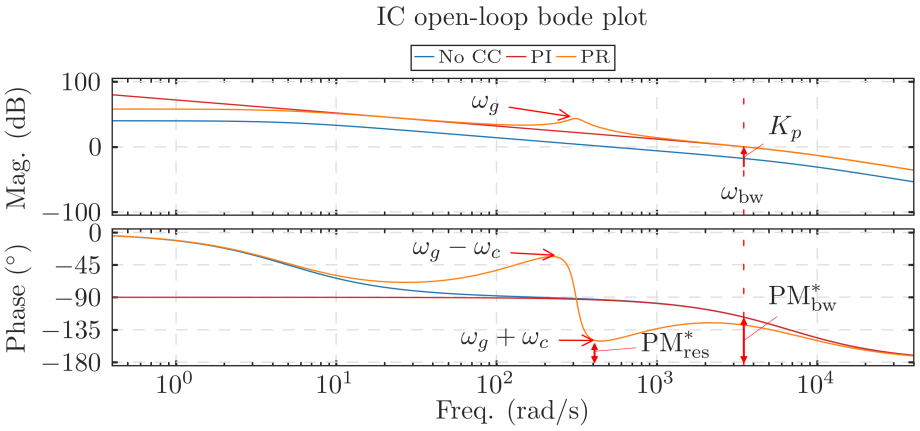

Figure 1.14 Bode plot of the IC open-loop of a generic system when no current control is applied, when a PI controller is applied and when a non-ideal PR controller is applied.

Lastly, the value of K_r can be obtained by making the minimum desired phase margin of the open-loop around the resonant frequency (PM^*_{res}) to be within $[30,60]^\circ$. Considering the output phase of PR controllers, the minimum phase margin is given immediately after the resonant frequency ω_r (see Fig. 1.8, where a peak of -90° is given on the right hand side of ω_g). Similarly, with non-ideal PR controllers, where the bandwidth is widened by ω_c, the minimum phase is given at $\omega_r + \omega_c$. Therefore, making

$$\angle G_{\text{IC}_{\text{ol}}}(j(\omega_r + \omega_c)) = \pi - \text{PM}^*_{\text{res}} \frac{2\pi}{360}, \tag{1.46}$$

would result in a design value for K_r. It is worth mentioning that, for non-ideal resonant controllers, the cut-off frequency ω_c for grid-connected converters is recommended to be selected in the range of 5-15 rad/s [41].

A tuning process example using a Bode plot is shown in Fig. 1.14, where the IC open-loop Bode plot of a generic system is shown when no current controller (CC) is implemented. Firstly, the value of ω_{bw} is determined in such a way that PM^*_{bw} is achieved for that frequency. At this point, it is common to assume that the resonant term would have no effect on the phase output, despite the fact that the figure shows that the resonant term adds a slight phase-shift at ω_{bw}. Afterwards, the value of K_p is determined to make ω_{bw} the crossover frequency of the open loop. Lastly, K_r is designed to achieve PM^*_{res} in the lowest phase around ω_g. Note that this model uses a non-ideal resonant controller. Additionally, the open-loop Bode plot when a PI is used is also included. In this case, the K_p and ω_{bw} tuning process follows the same procedure, and K_i is obtained through making $T_i = T_c$ as mentioned in (1.42).

dc-link voltage controller

Using the simplified model of the inner control loop in (1.25),

$$G_{\mathrm{OC_{ol}}}(s) = \frac{(K_p s + K_i)}{s^2 V_{dc} C(1+3T_s s)} = \frac{K_p(1+T_i s)}{T_i s^2 V_{dc} C(1+3T_s s)}, \quad T_i = \frac{K_p}{K_i}, \tag{1.47}$$

where T_i is the integral time constant. It is worth mentioning that the value of T_i should be tuned to be much larger than the IC time constant. Then, the crossover frequency of $G_{\mathrm{OC_{ol}}}(s)$ can be designed to be $\omega_{\mathrm{co}} = 1/\sqrt{3T_s T_i}$, as the maximum phase margin will be obtained. Therefore, the control parameters are given by

$$K_p = \frac{V_{dc} C}{\sqrt{3T_s T_i}}, \; K_i = \frac{V_{dc} C}{\sqrt{3T_s T_i^3}} \tag{1.48}$$

where the integral time constant T_i has to be tuned in such a way that the controller bandwidth lies between $1/50$ and $1/10$ of the one of the inner control loop, i.e $\omega_{\mathrm{co}} \approx \alpha/(3T_s)$ with $\alpha \in [1/10, 1/50]$.

Alternatively, [42] addresses this tuning process from several practical perspectives.

1.2.5 Current controller for unbalanced grid voltage conditions

It is also worth mentioning that the above analysis is based on a balanced three-phase grid. However an unbalanced three-phase grid voltage may require further considerations in terms of frequency response of the inner control loop. There are some unbalancing compensation strategies that inject non-fundamental components in the current references, and thus, the current controller must be able to track such components.

In this regard, [43] reviews the stationary and synchronous current control reference frames for these particular conditions of the electrical grid, and presents a theoretical comparison of the two current controllers explained above and others recently published.

This section will exhibit the characteristics of an unbalanced grid, how it is tackled from the control perspective of the converter, and some current controllers that are suitable to work under these grid conditions.

Unbalanced grid voltage conditions

A balanced three-phase grid is composed of three symmetrical sinusoidal voltage components with the same amplitude that are 120°-shifted between each other. In that case, their expressions are

$$v_{ga} = V_m \sin(\omega_g t), \quad v_{gb} = V_m \sin(\omega_g t - \frac{2\pi}{3}), \quad v_{gc} = V_m \sin(\omega_g t + \frac{2\pi}{3}), \tag{1.49}$$

where V_m is the voltage amplitude, and ω_g is the grid frequency in rad/s. However, the parasitic resistance of the transmission lines, non-linear characteristic of the loads, different kind of faults, and the unmatched power demand of each phase make a real three-phase grid to present an unbalanced distribution, that is, the previous assumptions are no longer true. Some reasons about why it is important to keep a grid balanced are the following:

- The sensitivity of certain grid-connected equipments that work under a limited range of voltage and frequency.
- Some topologies of drives are synchronized with the grid frequency, and therefore, its performance is highly dependant on the state of the grid balance.
- It is common to provide household costumers with single-phase energy, therefore an unbalance could make one or more phases to fail in the proper supply.
- Additional losses are generated the larger the unbalance is. For example, the common component, i.e. the component that results from adding the three-phases, is a well-known source of additional heating for many drives used in the industry.

In fact, the grid code standard defines a certain range of allowed unbalance, out of which, the supply might be suspended until the source of the unbalance is corrected.

A common approach to model such unbalance is by considering the Fortesque theorem. It states that any set of N unbalanced phasors—a vector with magnitude and phase—can be expressed as the sum of N symmetrical sets of balanced phasors, for values of N that are prime [44]. In this way, any unbalanced three-phase grid voltage can be expressed as the addition of a set of three balanced positive-sequenced voltages, a set of three balanced negative-sequenced voltages, and a set of three zero-sequenced voltages. That is,

$$\begin{aligned}\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} &= \begin{bmatrix} V_a \sin(\omega_g t + \phi_a) \\ V_b \sin(\omega_g t + \phi_b) \\ V_c \sin(\omega_g t + \phi_c) \end{bmatrix} \\ &= \underbrace{\begin{bmatrix} V_p \sin(\omega_g t + \phi_p) \\ V_p \sin(\omega_g t + \phi_p - \frac{2\pi}{3}) \\ V_p \sin(\omega_g t + \phi_p + \frac{2\pi}{3}) \end{bmatrix}}_{\text{Positive}} + \underbrace{\begin{bmatrix} V_n \sin(-\omega_g t + \phi_n) \\ V_n \sin(-\omega_g t + \phi_n + \frac{2\pi}{3}) \\ V_n \sin(-\omega_g t + \phi_n - \frac{2\pi}{3}) \end{bmatrix}}_{\text{Negative}} + \underbrace{\begin{bmatrix} V_z \\ V_z \\ V_z \end{bmatrix}}_{\text{Zero}},\end{aligned} \tag{1.50}$$

where V_a, V_b, V_c and ϕ_a, ϕ_b, ϕ_c are the respective individual amplitude and phase of each phase a,b,c; whereas V_p, V_n, V_z and ϕ_p, ϕ_n are the respective amplitude and phases of the balanced phasors in positive, negative and zero sequence. The zero sequence is also referred as common or homopolar component in the literature. With this representation, the ideal scenario is where $V_n = 0$ and $V_z = 0$, and thus, some approaches attempt to compensate the presence of the negative and zero component in such a way that only positive sequence appear in the voltage grid.

It is worth mentioning that, despite the formulation (1.50) that has been given for grid voltages, a similar decomposition can be applied to any three-phase variables: phase currents, voltage and current harmonics, etc.

Current reference generation for unbalanced grids

The only way a VSC can modify the grid voltage at the point of common coupling (PCC) is by interacting with the grid impedance using the injected phase currents. Considering that the flow of current through an impedance generates a voltage drop, the phase currents can be modified accordingly to generate a voltage drop that benefits the unbalance compensation of the grid voltage at the PCC. That is, from the VSC, to inject a certain phase current

waveform into the grid that interacts with the existing impedance between the VSC and the PCC in such a way that the voltage drop compensates in some extent the negative and zero sequence detected at the PCC. Generally, these strategies are implemented in VSCs working as rectifiers.

Recalling the instantaneous power theory [37], which establishes the relation between the instantaneous active and reactive power and the grid voltages and currents, the presence of negative or zero sequence components in the grid affects the power variables as well. Indeed, a balanced phase currents with unbalanced grid voltages yield fluctuations in the power flows. Nonetheless, in a three-phase three-wire system there is no presence of zero sequence as the Kirchhoff's law has to be fulfilled, i.e. $i_a + i_b + i_c = 0$. Applying the same sequence decomposition given in (1.50) to the phase currents—using I_p,I_n,I_z and $\sigma_p, \sigma_n, \sigma_z$ as the positive, negative and zero sequence amplitude and phase of the currents, respectively—, and expanding the instantaneous active power expression,

$$\begin{aligned}
p =& v_{ga} i_a + v_{gb} i_b + v_{gc} i_c = \frac{3}{2}(I_p V_p \cos(\phi_p - \sigma_p) + I_n V_n \cos(\phi_n - \sigma_n) \\
&+ I_p V_n \cos(\phi_n - \sigma_p - 2\omega_g t) + I_n V_p \cos(\phi_p - \sigma_n + 2\omega_g t)) \\
=& \frac{3}{2}(I_p V_p \psi_{pp} + I_n V_n \psi_{nn} \\
&+ I_p V_n (\psi_{np} \cos(2\omega_g t) + \varphi_{np} \sin(2\omega_g t)) \\
&+ I_n V_p (\psi_{pn} \cos(2\omega_g t) - \varphi_{pn} \sin(2\omega_g t)) \qquad (1.51) \\
\psi_{pp} =& \cos(\phi_p - \sigma_p); \quad \psi_{nn} = \cos(\phi_n - \sigma_n); \quad \psi_{np} = \cos(\phi_n - \sigma_p) \\
\varphi_{np} =& \sin(\phi_n - \sigma_p); \quad \psi_{pn} = \cos(\phi_p - \sigma_n); \quad \varphi_{pn} = \sin(\phi_p - \sigma_n)
\end{aligned}$$

where the zero sequence has been neglected given the explanation above. Note from (1.51) that the presence of a negative sequence component, whether in the voltages ($V_n \neq 0$) or phase currents ($I_n \neq 0$), generates oscillations in the active power at twice the grid frequency. The same conclusion can be applied to the instantaneous reactive power given that $q = v'_{ga} i_a + v'_{gb} i_b + v'_{gc} i_c$, where v'_{gi} refers to the 90°-lagged version of v_{gi} [45].

Using (1.51) and its analogue for the reactive power, the current reference generation stage can be adapted to take the presence of negative sequence in the grid voltage into account. It is worth mentioning that expression (1.51), applied to q as well, can be translated to the synchronous reference frame dq as

$$\begin{aligned}
p =& \frac{3}{2}((v_{gdq_p})^T i_{dq_p} + (v_{gdq_n})^T i_{dq_n} \\
&+ ((v_{gdq_p})^T i_{dq_n} + (v_{gdq_n})^T i_{dq_p}) \cos(2\omega_g t) \\
&+ ((J v_{gdq_p})^T i_{dq_n} + (v_{gdq_n})^T J i_{dq_p}) \sin(2\omega_g t)) \qquad (1.52) \\
q =& \frac{3}{2}((v_{gdq_p})^T J i_{dq_p} - (v_{gdq_n})^T J i_{dq_n} \\
&+ ((v_{gdq_p})^T J i_{dq_n} - (v_{gdq_n})^T J i_{dq_p}) \cos(2\omega_g t) \\
&+ ((v_{gdq_p})^T i_{dq_n} + (v_{gdq_n})^T i_{dq_p}) \sin(2\omega_g t)) \qquad (1.53)
\end{aligned}$$

$$J = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}.$$

Thus, an unbalanced set of references for a three-phase three-wire system in synchronous reference is composed of four variables: $i_{d_p}^*, i_{q_p}^*, i_{d_n}^*, i_{q_n}^*$. In the following, several strategies that have been developed in the literature to generate these references pursuing different objectives will be presented.

The easiest approach, commonly carried out in microgrids and transmission networks where the effect of grid impedances is more noticeable, is known as the droop control [46]. This technique is more focused on compensating voltage unbalances generated due to grid faults and it only uses positive-sequenced phase currents, i.e. the negative sequence component references are zero. By modifying the reactive power that flows through the line, the phase currents interact with the grid impedance, compensating the voltage drop. This strategy can be formulated as

$$\begin{aligned} i_{q_p}^* &= K_{\text{droop}} |V_{\text{nom}} - \min(V_a, V_b, V_c)| \cdot I_{\text{nom}} \\ K_{\text{droop}} &\geq 2, \end{aligned} \tag{1.54}$$

where K_{droop} is a fixed value that acts as a control parameter, min is the minimum function, and V_{nom} and I_{nom} are the nominal phase voltage of the grid—the desired value—and the nominal current of the VSC. Note that i_{q_p} is directly related to the reactive power, and therefore this strategy modifies the reactive power reference to compensate the voltage unbalance. Despite the fact that this is a common strategy, it does not take into account the presence of negative sequence components in the grid.

Another approach given in [45] considers an unbalanced input impedance—the impedance between the PCC and the VSC connection—and unbalanced grid voltage to formulate the instantaneous active and reactive powers using the so-called unified VSC model. For this, the expressions of the power oscillations at twice the grid frequency are presented as a function of the positive and negative sequence components of the grid voltages and phase currents, and the impedance parameters. This reference also exposes the fact that the expression that multiplies $\cos(2\omega_g t)$ in p has the same magnitude than the one that multiplies $\sin(2\omega_g t)$ in q, and similarly occurs with the term that multiplies $\sin(2\omega_g t)$ in p and the one that multiplies $\cos(2\omega_g t)$ in q (see (1.52)–(1.53)). In the latter case, both have the same magnitude but opposite signs. Therefore, considering the four degrees of freedom of the current references, four objectives are established:

- Fulfilling $p = p^*$.
- Fulfilling $q = q^*$.
- Cancelling the expression that multiplies $\cos(2\omega_g t)$ in (1.52).
- Cancelling the expression that multiplies $\sin(2\omega_g t)$ in (1.53).

As a result, the current references $i_{d_p}^*, i_{q_p}^*, i_{d_n}^*, i_{q_n}^*$ are obtained—set of equations expressed in (39) in work [45].

This current reference generation method exploits the benefits of defining the current references with no constraints as both power ripples are suppressed. However, harmonics

at $3\omega_g$ and $5\omega_g$ will be present in the grid current references. Consequently, the phase current references would not only have positive and negative sequence components, but also harmonics at those frequencies. Additionally, these harmonics have to be properly tracked by the current controller to fulfill the power oscillation suppression, which is an additional challenge for the current control design. Nevertheless, [45] proposes the use of parallel resonant controllers tuned at these frequencies for such purpose.

Alternatively, [47] defines a current reference generation strategy where the main objective is the voltage support at the PCC, i.e. the reduction of the negative sequence component in the grid voltage. This reference is based on the proposal given in [48], where the developed analysis is based on a mainly inductive transmission network, and thus it is expected that the phase currents interact with the grid inductance to provide voltage support. In contrast, authors in [47] expand the same analysis by taking into account the resistive-inductive ratio (R/X) of the network—while high-voltage networks are mainly inductive ($R/X = 0$), low-voltage networks are mainly resistive ($R/X \gg 0$). Nonetheless, both strategies present two inter-dependant tuning parameters k^+ and $k^- = 1 - k^+$, that act as weighting factors on which voltage sequence to consider for the current reference generation. The expressions are given in the $\alpha\beta$ reference frame as

$$i_\alpha^* = \frac{2}{3}p^* \frac{k^+ v_{g\alpha_p} + \frac{R}{\sqrt{R^2+X^2}}(k^- v_{g\alpha_n})}{k^+ V_p^2 + \frac{R}{\sqrt{R^2+X^2}}(k^- V_n^2)} + \frac{2}{3}q^* \frac{k^+ v_{g\beta_p} + \frac{X}{\sqrt{R^2+X^2}}(k^- v_{g\beta_n})}{k^+ V_p^2 + \frac{X}{\sqrt{R^2+X^2}}(k^- V_n^2)} \tag{1.55}$$

$$i_\beta^* = \frac{2}{3}p^* \frac{k^+ v_{g\beta_p} + \frac{R}{\sqrt{R^2+X^2}}(k^- v_{g\beta_n})}{k^+ V_p^2 + \frac{R}{\sqrt{R^2+X^2}}(k^- V_n^2)} + \frac{2}{3}q^* \frac{-k^+ v_{g\alpha_p} - \frac{X}{\sqrt{R^2+X^2}}(k^- v_{g\alpha_n})}{k^+ V_p^2 + \frac{X}{\sqrt{R^2+X^2}}(k^- V_n^2)}, \tag{1.56}$$

where $v_{g\alpha_p}, v_{g\beta_p}, v_{g\alpha_n}, v_{g\beta_n}$ are the $\alpha\beta$ instantaneous grid voltage values for positive and negative sequences, respectively; whereas R and X are the estimated resistance and inductance between the VSC and the PCC. In this way, parameters k^+ and k^- allow the current reference strategy to tune the amount of negative sequence current injected to the grid to provide voltage support: $k^+ = 1$ generates balanced phase currents not providing any voltage support, whereas lower values of k^+ increases the negative sequence current injection that interacts with the network impedance providing grid voltage equalization.

Sect. VII of work [49] presents the current reference expressions for the negative sequence under different scenarios of grid faults. These expressions are given in the dq reference frame and they aim to neglect the active power ripple in order to avoid ripples in the dc-link voltage. Alternatively, [50] defines two simple current reference generation strategies: the first one aims to provide the desired power with no negative sequence current, while the second one aims to reduce the active power oscillation by means of injecting negative sequence current. Similarly, authors in [51] expand this idea by using a tuning parameter $K \in [-1,1]$ that weights between three possible objectives: reactive power ripple suppression ($K = -1$), only positive sequence currents ($K = 0$), and active power ripple suppression ($K = 1$). The expressions derived for the current reference

obtention are the followings

$$\begin{bmatrix} i^*_{d_p} \\ i^*_{q_p} \\ i^*_{d_n} \\ i^*_{q_n} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} v_{gd_p}/D & v_{gq_p}/E \\ v_{gq_p}/D & -v_{gd_p}/E \\ v_{gd_n}/D & v_{gq_n}/E \\ v_{gq_n}/D & -v_{gd_n}/E \end{bmatrix} \begin{bmatrix} p^* \\ q^* \end{bmatrix} \tag{1.57}$$
$$D = v^2_{gd_p} + v^2_{gq_p} - K(v^2_{gd_n} + v^2_{gq_n})$$
$$E = v^2_{gd_p} + v^2_{gq_p} + K(v^2_{gd_n} + v^2_{gq_n}).$$

Note that making $K = 0$ is equivalent to the first strategy presented in [50], while making $K = 1$ is equivalent to its second strategy.

Similar to the previous method, depending on the aimed objective, [52] tunes the conductance g and susceptance b for each sequence to determine the current references from its corresponding grid voltage. That is, the values of g^+, g^-, b^+ and b^- are tuned depending on the pursued objective: active power ripple suppression, reactive power ripple suppression, or balanced phase currents. Defining the relation between the negative and positive susceptance and conductance respectively as $k_g = g^-/g^+$, $k_b = b^-/b^+$, the reference currents are defined

$$i^*_{dq_p} = g^+ v_{gdq_p} - Jb^+ v_{gdq_p} \tag{1.58}$$
$$i^*_{dq_n} = k_g g^+ v_{gdq_n} - Jk_b b^+ v_{gdq_n} \tag{1.59}$$
$$g^+ = \frac{2}{3}\frac{p}{V_p^2 + k_g V_n^2}\,; \quad b^+ = \frac{2}{3}\frac{q}{V_p^2 + k_b V_n^2}\,,$$

where it can be seen that a similar expression than the one shown in (1.57) is given. Indeed, parameters k_g and k_b can be fixed to pursue the same objectives than the previous strategies: $k_g = -1, k_b = 1$ yields no active power ripple, $k_g = 1, k_b = -1$ yields no reactive power ripple, and $k_g = 0, k_b = 0$ yields balanced phase currents. In contrast to [51], there is an additional degree of freedom given the fact that there are two parameters to be tuned. This degree of freedom is used in this paper to carry out a current limitation strategy where the maximum amplitude of the phase currents is managed by clamping both k_g and k_b during online operation.

Current controllers for unbalanced grid conditions

Some of the previous strategies that provide voltage support define a nonzero magnitude for the negative sequence components of the current references ($i^*_{dq_n} \neq 0$). Then, it is expected that the current controller (CC) can track such magnitude when implemented in a closed-loop scheme.

For the balanced case, where only positive sequence components of the current references are given, two common CCs were previously explained: the PI controller using synchronous reference frame, and the PR Controller using stationary reference frame. These controllers are valid to track DC magnitudes, in the case of the PI-based, and AC magnitudes at a specific frequency, for the PR-based. However, in the case of unbalanced

grid voltage, the existence of negative sequence components in the current references requires the frequency response of the CC to offer a high gain at this negative frequency in order to achieve negative-sequence tracking capabilities.

CCs in synchronous reference frame

In order to implement the PI controller as a CC, the synchronous reference frame dq is used, where the AC magnitudes at the fundamental frequency are transformed to DC magnitudes by means of using a rotating reference frame. However, given that this transformation implies a rotation at the fundamental frequency ω_g, any other AC magnitude with different frequency ω is seen in the synchronous reference frame as an AC magnitude with frequency $\omega - \omega_g$. Then, the negative sequence component appears in the synchronous reference frame as an AC magnitude at $2\omega_g$, and thus the PI controller alone does not suffice to track this magnitude. In this regard, several CC strategies have been proposed in the dq reference frame.

Double synchronous reference frame

One approach is to use the concept of double synchronous reference frame where the positive and negative sequence components are treated separately as DC magnitudes. Firstly, the measured currents in abc are transformed using two synchronous reference frames: the positive sequence reference frame rotates counter-clockwise (and thus $T_{abc\rightarrow dq}(\theta)$ is applied), whereas the negative sequence reference frame rotates clockwise (and thus $T_{abc\rightarrow dq}(-\theta)$ is applied). Afterwards, the $2\omega_g$ oscillations that appear in each reference frame due to the opposite component presence should be eliminated. One way is by means of a low-pass filter, but it also filters out the reference components that are above the cut-off frequency and limits the closed-loop control response. Alternatively, notch filters tuned at $2\omega_g$ are an effective way to get rid of this specific frequency. In any case, the phase currents, initially measured in abc as AC magnitudes, are separated into the positive and negative sequence components as DC magnitudes in each synchronous reference frame. This process can be expressed mathematically as follows

$$\begin{bmatrix} i_{d_p} \\ i_{q_p} \end{bmatrix} = \text{Filter}\left(T_{abc\rightarrow dq}(\omega_g t) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \right); \quad \begin{bmatrix} i_{d_n} \\ i_{q_n} \end{bmatrix} = \text{Filter}\left(T_{abc\rightarrow dq}(-\omega_g t) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \right),$$

where Filter is the function that represents the used filter. This process is also known as current decomposition or current sequence separation. Hence, the common strategy of using a PI controller to regulate the currents can be adopted as both sequences are DC magnitudes. Consequently, the double synchronous reference frame uses four PI controllers, two for each component in the positive and negative sequence reference frames [53]. It is worth mentioning that the requirement of the sequence current separation stage introduces additional delays and undesired resonances into the closed-loop control. That is why, some works aimed to implement the same strategy of the double synchronous reference frame but neglecting the sequence current extraction stage as it will be shown later in this section.

As an alternative, [53] uses the so-called decoupled dual synchronous reference frame where the ripples from each component are subtracted by means of low-pass filtering and

rotating the opposite component magnitude. Thanks to this, the required filter is not placed in the forward path of the currents, and it is translated as a feedback path to uncouple each sequence from the opposite. In this way, the dynamic limitation of (1.2.5) is avoided. The expression for this sequence current decomposition is the following

$$\begin{bmatrix} i_{d_p} \\ i_{q_p} \end{bmatrix} = T_{abc\to dq}(\omega_g t) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - L_{\text{rot}}(2\omega_g t)\text{LPF}\left(\begin{bmatrix} i_{d_n} \\ i_{q_n} \end{bmatrix} \right) \tag{1.60}$$

$$\begin{bmatrix} i_{d_n} \\ i_{q_n} \end{bmatrix} = T_{abc\to dq}(-\omega_g t) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - L_{\text{rot}}(-2\omega_g t)\text{LPF}\left(\begin{bmatrix} i_{d_p} \\ i_{q_p} \end{bmatrix} \right), \tag{1.61}$$

where LPF refers to the low-pass filter function, and $L_{\text{rot}}(\theta)$ refers to the rotation matrix given in (1.17). Note that the bandwidth of each LPF has to be tuned below the $2\omega_g$ ripple in such a way that only the DC magnitude is extracted. Therefore, the current references can be properly tracked by means of PI controllers.

Another alternative presented in [51] avoids the sequence current decomposition stage while still using the two sequence reference frames. However, instead of considering the references as pure DC magnitudes, it adds the opposite sequence current references. That is,

$$\begin{bmatrix} i^*_{d_p} \\ i^*_{q_p} \end{bmatrix}' = i^*_{dq_p} + L_{\text{rot}}(2\omega_g t) i^*_{dq_n} \tag{1.62}$$

$$\begin{bmatrix} i^*_{d_n} \\ i^*_{q_n} \end{bmatrix}' = i^*_{dq_n} + L_{\text{rot}}(-2\omega_g t) i^*_{dq_p} \tag{1.63}$$

where ${i^*_{dq_p}}'$, ${i^*_{dq_n}}'$ are the computed references with the opposite sequence included that input the CC. This approach skips the sequence current decomposition while still keeping uncoupled the positive sequence component control from the negative one. Note that this approach has ideally the same effect at steady-state on the current tracking error $\widetilde{i_{dq}} = i^*_{dq} - i_{dq}$ than the one presented in (1.60)–(1.61), as $\text{LPF}(i_{dq_p}) = i^*_{dq_p}$ and $\text{LPF}(i_{dq_n}) = i^*_{dq_n}$ are fulfilled whenever the current tracking is properly achieved. Consequently, an oscillatory term $(2\omega_g t)$ is added to the references. However, the controller is not required to track it, as it is an oscillation that will appear in the current magnitudes given that the opposite sequence DC magnitude is properly tracked. Due to this, PI controllers in the double synchronous reference frame are still good candidates to achieve proper tracking of both positive and negative sequence components. In [51], the closed-loop behaviour of this proposal is analyzed in such a way that the maximum possible gains for the PI controllers are obtained.

Lastly, the CC presented in [54] ignores the current reference of the negative sequence components, but instead it tries to compensate the dc-link voltage oscillation. For this purpose, an AC signal with amplitude M_{AC}, phase α_{AC} and frequency $2\omega_g$ is added to the angle of the output voltage vector v_{dq} to be modulated. The amplitude M_{AC} is computed from the extracted negative sequence components of the currents—using the

negative synchronous reference frame plus a notch-filter to reject the $2\omega_g$ ripples—which later inputs a PI controller. The term $\cos(2\omega_g t + \alpha_{\text{AC}})$ is computed from the $2\omega_g$ ripple extracted from the positive sequence reference frame by means of another notch filter. It is later proved that this oscillation in the output angle compensates for the active power ripple, and thus the dc-link voltage oscillation.

Single synchronous reference frame

Alternatively to using two synchronous reference frames, PI controllers along with resonant terms can be used to track specific harmonics [33,55] in only one reference frame. In this regard, the negative sequence component appears in the positive synchronous reference frame as a magnitude at $2\omega_g$, and therefore a resonant term at this frequency can be used to achieve tracking capability. Thus, by using (1.62) to integrate both sequence references into one, the previously presented synchronous scheme with PI controller can be used with the addition of a resonant term tuned at $2\omega_g$.

$$\begin{bmatrix} i^*_{d_p} \\ i^*_{q_p} \end{bmatrix}' = \underbrace{i^*_{dq_p}}_{\text{DC magn.}} + \underbrace{L_{\text{rot}}(2\omega_g t)\ \overbrace{i^*_{dq_n}}^{\text{DC magn.}}}_{\text{AC magn.}} \tag{1.64}$$

In contrast to [51], this method uses two PI controllers to track the DC magnitudes of i'_{dq_p}, and two resonant terms to track the AC magnitudes, while using only one synchronous reference frame. This scheme can be potentially used to track other harmonic references or to neglect their appearance in the current output. However, it is necessary to consider that a positive harmonic $n\omega_g$ would appear in the positive synchronous reference frame as a $(n-1)\omega_g$ harmonic, while a negative harmonic $n\omega_g$ would appear as a $(n+1)\omega_g$ one. Given that the typical low-order harmonics, the 5th and 7th ones, are respectively negative and positive sequences, they appear in the synchronous reference frame as a $-6\omega_g$ and a $6\omega_g$ components. Therefore, two resonant terms are required in order to track/compensate such components.

Following the scheme of PI+Res in single reference frame for positive and negative sequence tracking, the CC transfer function results in

$$C_{\text{C}}(s) = K_p + \frac{K_i}{s} + \frac{K_r s}{s^2 + 4\omega_g^2} = \frac{(s^2 + 4\omega_g^2)(K_p s + K_i) + K_r s}{s(s^2 + 4\omega_g^2)}, \tag{1.65}$$

which applied to the closed-loop transfer function given in (1.34) yields

$$G_{\text{IC}_{\text{cl}}}(s) = \frac{((s^2 + 4\omega_g^2)(K_p s + K_i) + K_r s)T_c}{L(1 + 1.5T_s s)(1 + T_c s)s(s^2 + 4\omega_g^2) + ((s^2 + 4\omega_g^2)(K_p s + K_i) + K_r s)T_c}. \tag{1.66}$$

Using (1.13), the closed-loop transfer function $D_{\text{IC}_{\text{cl}}}(s)$ results in

$$D_{\text{IC}_{\text{cl}}}(s) = \frac{s(s^2+4\omega_g^2)T_c}{L(1+1.5T_s s)(1+T_c s)s(s^2+4\omega_g^2)+((s^2+4\omega_g^2)(K_p s+K_i)+K_r s)T_c}. \tag{1.67}$$

In order to depict the frequency response of such controller, the same control parameters exhibited in Sect. 1.2.4 are used and the Bode plot of both transfer functions, when using only a PR controller ($K_i = 0$) and PI+Res ($K_i \neq 0$) controller, are depicted in Fig. 1.15. It is shown that $G_{\text{IC}_{\text{cl}}}(s)$ gives 0 dB and 0° at twice the grid frequency (100 Hz) thanks to the PR controller. However, the integral term is required to guarantee 0 dB for DC magnitudes. Therefore, under a positive sequence synchronous reference frame, the integral term tracks the positive sequence component (DC magnitudes) and the resonant term tracks the negative sequence component (AC magnitudes). Additionally, it is shown that the PI+Res scheme tend to offer a $-\infty$ magnitude for distortions at DC and $2\omega_g$ in the control signal, which validates the disturbance rejection in the grid voltage feedforward variable used in the inner control loop.

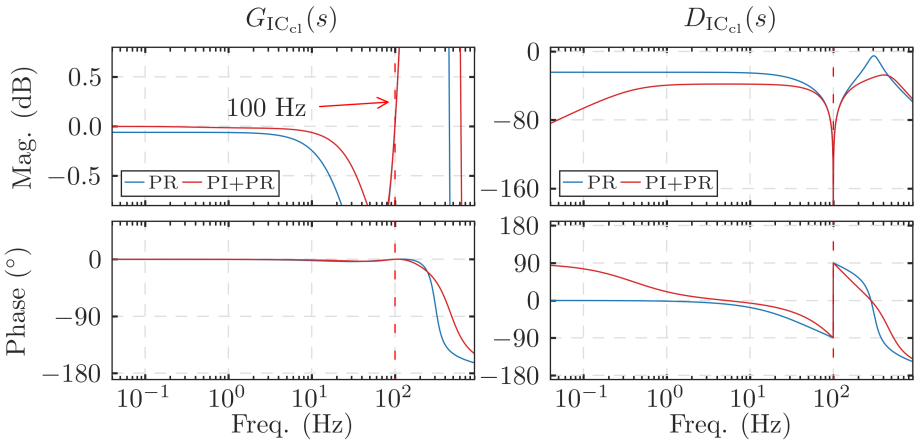

Figure 1.15 Bode diagram of transfer functions shown in (1.66) and (1.67) for $K_i = 0$ (PR) and $K_i \neq 0$ (PI+PR).

This same work [33] also exhibits that having the PLL—which will provide the angle $\omega_g t$ to be used for the transformation to the synchronous frame—fed with the voltage grid with some casual harmonic content, makes the PI controller to act as a resonant controller tuned at those frequencies in both positive and negative sequence components. This would assist in the rejection of the presence of these harmonics in the phase currents.

CCs in stationary reference frame

Contrary to all the above-mentioned CCs, other works, such as [45], keep the measured magnitudes in the stationary reference frame $\alpha\beta$ and implement PR controllers to track the AC sequence components that appear in the current references. As it was mentioned before, a PR controller in stationary frame is equivalent to two PI controllers in positive and negative synchronous reference frames [34]. Therefore, implementing a PR controller in $\alpha\beta$ tuned at ω_g is equivalent to the dual-synchronous reference frame mentioned previously. That is, a PR controller tuned at ω_g in $\alpha\beta$ is equivalent to a PI controller in a dq positive sequence synchronous reference frame and a PI controller in a dq negative sequence synchronous reference frame. Consequently, a PR controller can track the AC magnitudes ω_g and $-\omega_g$ simultaneously. Following the proposal given in [45], three resonant terms are tuned for the fundamental frequency, the 3rd harmonic and the 5th harmonic, resulting in the CC transfer function

$$\begin{aligned} C_{\mathrm{C}}(s) &= K_p + \frac{K_r s}{s^2+\omega_g^2} + \frac{K_r s}{s^2+(3\omega_g)^2} + \frac{K_r s}{s^2+(5\omega_g)^2} \\ &= \frac{N_c(s)}{(s^2+\omega_g^2)(s^2+(3\omega_g)^2)(s^2+(5\omega_g)^2)}. \end{aligned} \tag{1.68}$$

Substituting $C_{\mathrm{C}}(s)$ in the closed-loop transfer function given in (1.34),

$$G_{\mathrm{IC_{cl}}}(s) = \frac{N_c(s)T_c}{L(1+1.5T_s s)(1+T_c s)(s^2+\omega_g^2)(s^2+(3\omega_g)^2)(s^2+(5\omega_g)^2)+N_c(s)T_c}. \tag{1.69}$$

Similarly, the closed-loop transfer function for distortions in the control signal given in (1.13), can be obtained as follows

$$D_{\mathrm{IC_{cl}}}(s) = \frac{(s^2+\omega_g^2)(s^2+(3\omega_g)^2)(s^2+(5\omega_g)^2)T_c}{L(1+1.5T_s s)(1+T_c s)(s^2+\omega_g^2)(s^2+(3\omega_g)^2)(s^2+(5\omega_g)^2)+N_c(s)T_c}. \tag{1.70}$$

The Bode plot of both transfer functions are depicted in Fig. 1.16 using the same control parameters exhibited in Sect. 1.2.4. It can be seen that $G_{\mathrm{IC_{cl}}}(s)$ properly tracks the current references at 50, 150 and 250 Hz according to the control design as it gives 0 dB and 0° at those frequencies. Additionally, $D_{\mathrm{IC_{cl}}}$ tends to $-\infty$ dB and 0° at the same frequencies, which indicates that the presence of these harmonics in the grid voltage feedforward variable does not affect the current controller performance.

1.3 Background on multilevel power converters

The above sections are referred to grid-connected two-level converters, where each of the semiconductor devices have to support the full dc-link voltage when they are switched-off.

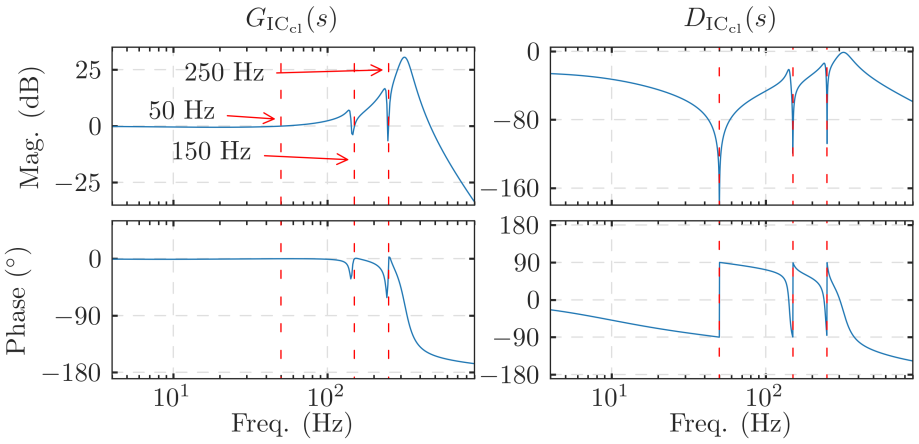

Figure 1.16 Bode diagrams of transfer functions shown in (1.69) and (1.70).

Recalling Fig. 1.2, if S_1^a is switched-on, point a is connected to the positive side of the dc-link, and thus the switching device governed by $\overline{S_1^a}$ has to stand the full dc-link voltage. This fact exhibits an important limitation for two-level converters as the voltage operation limits of the converter are dictated by the maximum voltage the semiconductor devices can stand. Considering this, two-level converters are not suitable for direct connection to some transmission lines, and thus they require a step-up AC/AC stage as an interface. This is specially deterrent for medium and high-power applications, such as offshore wind farms or large power drives, where the conducting losses derived from the insertion of the AC/AC stage considerably decreases the overall system efficiency. Moreover, those two-level converters that can stand these high voltages induce such large output voltage pulses that the size of the AC filter required to fulfill the grid code limits opposes the benefits of a direct connection.

Multilevel converters appear as a solution for the above-mentioned issues by using several switching devices in series [56]. The main idea is to divide the dc-link voltage in two or more levels in such a way that every output can be connected to each of these levels. The obtained benefits are twofold: the output voltage—v_{iN} in Fig. 1.2—resembles more accurately the fundamental signal to be modulated, and the switching devices no longer have to stand the whole dc-link voltage but the voltage difference between these levels. The latter allows the use of switching devices with lower voltage limits than that of the converter operating point, which are usually smaller, cheaper, more efficient and can manage larger switching frequencies. In summary, the potential advantages of multilevel converters are

1. Improved output current and voltage distortion.

2. Lower switching losses due to either the lower parasitic capacitance that smaller switching devices have, or the possibility of reducing the switching frequency while achieving the same output quality compared to the two-level topology.

3. Smaller passive filter components due to the reduction in the output distortion and switching frequency ripple.
4. Lower conducting losses in each switching device due to the reduced parasitic resistance and forward voltage that smaller switching devices have.
5. Reduced emission of electromagnetic interference.
6. Extension of the voltage limits of the system.

Despite these advantages, some issues arise in multilevel converters that must be tackled in the control design. The extension in the amount of available levels increases the complexity of the control as more switching configurations are possible. Additionally, as there are more than one DC voltage level, these levels do not necessarily remain equal. It is common that the voltage of each level is hold by a capacitor, and thus its voltage may change during normal operation if its power flow is not properly managed. This issue is commonly known as capacitor voltage balance. A common approach is to design strategies for the command of the switching devices, that is the modulation stage, in such a way that it takes this issue into account and provides one mean to guarantee the proper balance of these levels. Alternatively, some approaches aim to integrate the capacitor voltage balancing in the control stage as another control objective.

In the following, some topologies of multilevel converters will be shown. Then, several common carrier-based modulations for multilevel converters will be presented, along with a brief description of alternative modulation approaches.

1.3.1 Multilevel converter topologies

There exists plenty of topologies in the literature that has been reported since the 70s [57], each of them offering different features. A general classification given in [58] is made by considering the type of DC source; either they have a single DC source, where the whole system share the same dc-link, or individual DC sources, where the system is comprised of one or more cells that have their own dc-link. Some of the most common topologies are mentioned below.

Diode-clamped converters (DCC)

This topology of power converter incorporates switching devices and power diodes in such a way that the maximum voltage each semiconductor has to endure is divided by the number of levels $(n-1)$ [59]. Thus, a five-level DCC reduces the voltage stress of each device by four in comparison with the two-level version. This topology belongs to the first category, as the whole converter shares the same dc-link, which has to be divided into n levels by means of $n-1$ serialized capacitors. The principle of this converter is to have a switching configuration for every phase that connects the output to each of these dc-link levels. For a n-level DCC, $2(n-1)$ switching devices with an anti-parallel diode and $2(n-2)$ power diodes are required per phase. Whenever a level j is connected to the output, the phase current flows from or to that level in the dc-link. Therefore, it will generate an unbalance between the capacitor voltages, as there will be a mismatch between the power flowing through the capacitors above and below this level j. It is shown that, under normal operation, were this problem not to be taken into account and using

the simplest modulation approach—usually the two nearest level in PWM or the three closest vector in SVM—, the capacitor voltages would tend to diverge, causing an improper behaviour of the system, or even damaging the semiconductor devices [60]. Accordingly, taking advantage of the periodic nature of the phase voltages and currents, this issue can be modelled by measuring the current that inputs every level of the dc-link over a grid period [61].

The simplest topology inside this category is the well-known neutral point clamped (NPC) converter [62], which is the three-level version of the DCC. The NPC reduces the voltage each device has to stand by half in comparison with the two-level version working under the same dc-link voltage. The reduced complexity of this converter and its improvements in output distortion and voltage limits have made this converter very popular in medium-voltage industrial applications. Indeed, simple control laws have been developed [63] that take advantage of the multilevel nature of NPCs. The scheme of a three-level NPC configuration for a phase i is shown in the left-hand side of Fig. 1.17, whereas the five-level DCC configuration is shown in the right-hand side of the same figure.

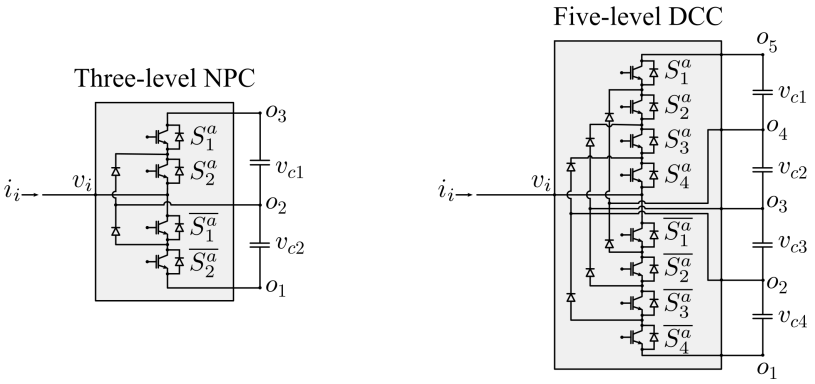

Figure 1.17 Scheme of the three-level (left) and five-level (right) DCC for one phase. Parallel connection of these schemes would build-up a n-phase system.

Despite the fact that three-level topology is broadly used, the topologies with four or more levels still find some reluctance to be adopted due to the accumulated increment in complexity and hardware. Nevertheless, there are still some efforts aimed at providing a simple control law for such configurations [64, 65]. This dissertation will present some contributions for the three- and five-level configurations.

Flying capacitor (FC)

Flying capacitor (FC) topology is relatively new compared to the DCC and, in spite of not being as typical as NPC, it offers some advantages over it, such as no need for additional power diodes, or additional degrees of freedom in the switching configuration selection [66]. The system has one dc-link and the main difference with the DCC is that the different levels are generated by controlling which capacitors are serialized—which are referred as flying capacitors. In this way, the resulting output voltage is the combination

of the dc-link voltage and the capacitor voltages. The three- and five-level schemes of one phase for a FC converter are shown in Fig. 1.18, where it can be deduced that a n-level FC converter requires $2(n-1)$ switching devices with an anti-parallel diode, and $n-1$ capacitors.

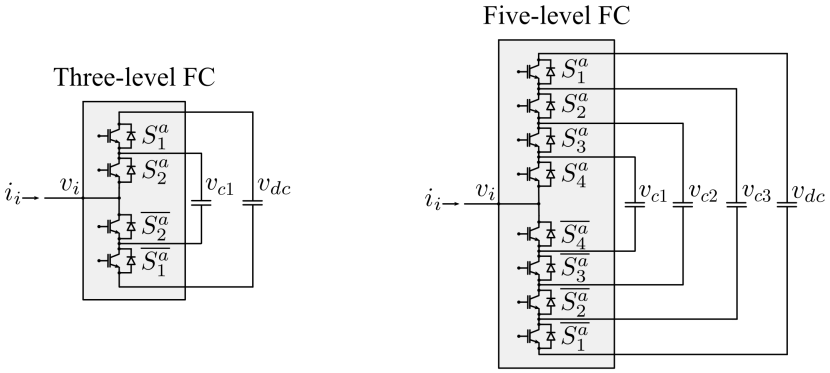

Figure 1.18 Scheme of the three-level (left) and five-level (right) FC converter for one phase. Parallel connection of these schemes would build-up a n-phase system.

The common approach for this topology is to regulate the capacitor voltages in such a way that there exist redundant switching configurations, i.e. some switching positions that achieve the same output voltage but with different current paths. Thus, the capacitor voltage balance can be achieved by using this redundancy. Additionally, one advantage of this topology is that it is possible to change the ratio of the capacitor voltages—the desired capacitor voltage relation—to increase the number of voltage levels sacrificing some redundancy in order to improve the output voltage distortion [67]. In this case, a trade-off between output distortion and capacitor voltage balancing is made explicit. Some works address this lack of redundancy in three-phase, three-wire system by means of joint redundancy, i.e. by modifying the common component of the three-phase voltages considering that the currents remain unaffected by it [68].

Using the three-level FC converter shown in Fig. 1.18 as reference guide and taking the negative side of the dc-link as reference point, having $S_1^a = 1$ and $S_2^a = 0$ would output $v_i = v_{dc} - v_{c1}$, whereas $S_1^a = 0$ and $S_2^a = 1$ would output $v_i = v_{c1}$. Thus, if v_{c1} is kept around $v_{dc}/2$, three possible levels are generated, and there are two switching states that provide the same output voltage but with different current paths, i.e. they are redundant states. Alternatively, if v_{c1} is kept around $v_{dc}/3$, there are four possible levels, but the balancing task is more difficult to achieve. It is also worth mentioning that the last case would make the voltage limits that some switching devices have to stand larger than others, increasing also the complexity of the design stage.

Regarding the voltage balancing, some works propose active balancing of such converters by modifying the duty ratios or including some strategies in the modulation scheme, among others [69]. Active balancing guarantees that each capacitor voltage reaches the desired value, however additional control loops are required for each considered capacitor. On the

contrary, passive balancing or natural balancing does not require a voltage sensor for each capacitor nor additional control loops by guaranteeing that the duty ratios of each level are evenly distributed [70]. With this, the power flow between different capacitors is naturally balanced, and the analysis of the system dynamics proves that any external disturbance would make the system to converge naturally to a balanced situation. Natural balancing is usually achieved by means of carrier-based modulations.

Cascaded and Modular converters

Cascaded converter refers to those multilevel configurations that are based on a serial connection of several single-phase converters [71]. In contrast to the previous topologies, each of these converters has its own dc-link, allowing the cascaded configuration to be seen as a serialized set of independent power modules. Some of the most obvious advantages are high modularity and scalability, easy maintenance, replication of control structure and modulation among power cells, and robust operation due to the possible inclusion of redundant power cells [72]. In spite of allowing the use of switching devices with much lower voltage rate, there is an obvious increase in the associated electronic, i.e. gating drives, optical signals, ADCs, etc., which may compromise the benefits of such converters. Needless to say that the power cells inside one phase can be of different topologies leading to hybrid cascaded configurations with some distinctive features of the involved power cells.

Regarding the redundancy in the output voltage generation, the power cells that have the same dc-link voltage can be switched indifferently, resulting in a more numerous amount of redundant switching vectors. In fact, it is common to use sorting algorithms that takes the DC voltage of each cell into account and indicate which cells should be prioritized in the connection according to the phase current. Nevertheless, the redundancy in these systems highly depends on the type of cells that are used. Moreover, there exists the so-called asymmetric cascaded converters where the power cells do not have the same dc-link voltage, and thus they can provide more voltage levels. Similarly to the previous FC topology, the use of asymmetric cascaded converters improves the output distortion while increases the complexity of the voltage balancing task.

The most typical cascaded converter is the cascaded H-bridge (CHB) converter, which consists of serialized H-bridge cells per phase, where each cell has its own dc-link—either an isolated dc-source or a capacitor. Fig. 1.19 (left) depicts a five-level CHB for one phase i. Given that each H-bridge can output the dc-link voltage positively and negatively, a n level CHB consists of $(n-1)/2$ H-bridge cells. In [73] an hybrid cascaded converter configuration is presented, which uses a single-phase multilevel VSI—usually DCC or FC topologies—as the dc-link of a H-bridge in such a way that the generated output of the VSI can be modulated positively and negatively thanks to the action of the H-bridge. This scheme is depcited in Fig. 1.19(center) for a generic phase i.

Alternatively to the cascaded converter, it is worth mentioning the modular multilevel converter (MMC) as it has become one of the most studied multilevel topology, specially for high-voltage direct current (HVDC) transmission systems. It shares the same principle of the cascaded converter by serializing DC/DC converters with isolated dc-links to provide either a single- or three-phase multilevel output voltage. In contrast to the CHB, the MMC is composed of two arms that connect the phase output with the positive and negative side

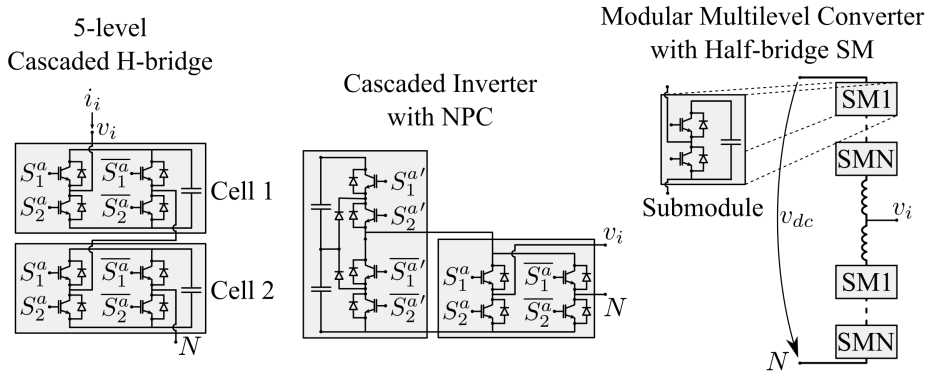

Figure 1.19 Scheme of two cascaded and one modular converters for one phase: Cascaded H-bridge converters (left), Cascaded inverter with an NPC in the dc-link (center), Modular multilevel converter with half-bridge Submodules (right). Parallel connection of these schemes would build-up a n-phase system.

of the dc-link respectively, and two buffer inductors that limit the passing current. The most common module used in MMC is the half-bridge circuit due to its reduced components and simple control. An scheme of a MMC with half-bridge submodules is shown in Fig. 1.19(right). Alternatively, H-bridge circuits, clamp-double circuits, three-level DCC or five-level cross-connected circuits are also considered as modules for MMCs [74].

1.3.2 Modulation approaches for multilevel power converters

This subsection shows some of the most common modulation approaches for multilevel converters, that is, the strategy in charge of commanding the gating of the switching devices. Recalling the modulation strategies exhibited in Sect. 1.2.3, a similar distribution can be made into carrier-based PWM, space vector modulation, and optimal PWM schemes.

Carrier-based PWM

Carrier-based PWM for multilevel converters are usually based on using several carriers in such a way that the comparison of the modulation signals with each carrier commands the generation of a level, output of a cell or gating of a switching device. Considering the existence of several carriers, their disposition is very determinant in the performance of the system. In this regard, two categories are generally considered: Phase-shift modulation (PS-PWM) and Level-shift modulation (LS-PWM). PS-PWM keeps the same amplitude of the carriers but shifts each additional carrier a certain angle in such a way that the switching signal generation are evenly distributed along the switching period. On the contrary, LS-PWM modifies the amplitude and bias of the carriers such that they are disposed at different levels covering the whole range of the modulating signal, which usually goes from $-(N-1)/2$ to $(N-1)/2$, being N the number of considered levels, when it is normalized with respect to $v_{dc}/(2N)$.

Particularly, the angle shift in PS-PWM, when using cascaded converters, depends on the type of power cells that is used. Assuming that unipolar modulation is used for

H-bridges—two carriers that are 180°-shifted command the four switching devices of each H-bridge—, each set of carriers is shifted $180°/M$, being M the number of used H-bridge cells. In contrast, MMCs with half-bridge submodules (SM)—only one carrier is required per SM—or H-bridge cells with bipolar modulation would shift each carrier $360°/M$. In other words, PS-PWM shifts the carriers "horizontally". For this, the power is distributed evenly between power cells as they are switched-on at the same frequency, which benefits the capacitor voltage balancing of cascaded or flying capacitor converters. Moreover, thanks to the phase-shift effect, the effective output switching frequency is $N-1$ times that of the power cells. The latter is taken into consideration to reduce the switching frequency of each power cell while keeping the same effective output switching frequency.

Approach LS-PWM, on the contrary, shifts the carriers "vertically" in such a way that there are $N-1$ carriers in a N-level converter, each carrier associated to a level. With this, the output is set to the level whose corresponding carrier is immediately below the modulation signal—the lowest level is output in the case all carriers are above. There exist some variations depending on the phase disposition of the carriers, i.e. the "horizontal" disposition [24]:

- Phase disposition (PD), where all carriers are in-phase.
- Alternative phase opposite disposition (APOD), where the carriers are alternatively 180°-shifted.
- Phase opposite disposition (POD), where the upper half carriers are in-phase, and the lower half are 180°-shifted.

The differences between these depend on the multilevel system, however PD offers the best output harmonic distortion, and POD are especially suitable for limiting the circulating current in MMCs [74].

While PS-PWM is more suited for CHB and FC due to its inherent power flow equalization, which in fact assists on the capacitor voltage balance (natural balancing), LS-PWM can be used for any multilevel converter. An example of both modulations is shown in Fig. 1.20 for a 7-level converter, where the modulation signal, carrier disposition, and output voltage is depicted. The harmonic spectrum of the output waveform is also shown in Fig. 1.21, where it can be seen that the LS-PWM offers an harmonic spectrum centered around the carrier frequency, whereas PS-PWM have lower values of harmonic magnitude but more spread. For this example, the modulation signal is a fundamental component at 50 Hz, with a modulation index of 0.9—an amplitude of $0.9 \cdot 3 = 2.7$—, which is properly modulated as it can be seen in the harmonic spectrum.

Space-vector modulation for multilevel power converters

Following the same principle than SVM for two-level converters, the control region, where all possible switching states are depicted (see Fig. 1.6), can be represented for multilevel converters. For this, the normalized value of the output voltage vector $x_{\alpha\beta}$ is considered as $x_{\alpha\beta} := v_{\alpha\beta}/(v_{dc}/(N-1))$, where N is the number of levels that the topology under consideration has. Similarly to the two-level topology, the switching vector represents the level to which each phase is connected in alphabetical order, e.g. '324'

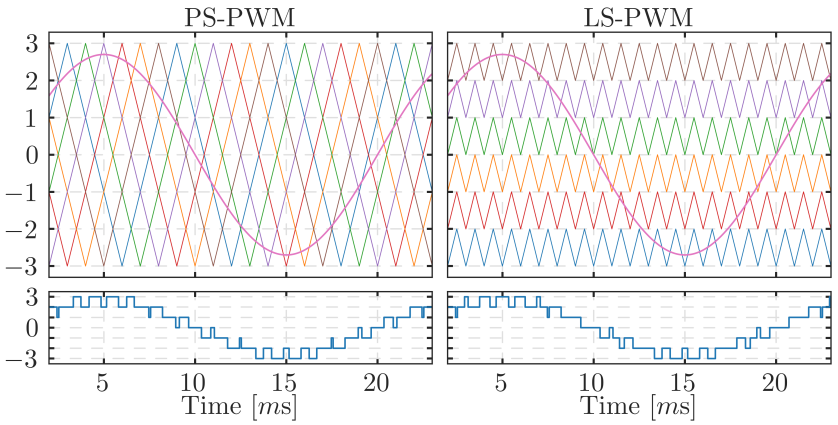

Figure 1.20 Phase- (left) and Level- (right) shift PWM approaches for a 7-level converter. PS-PWM have carriers with 1/7 kHz and LS-PWM with 1 kHz. The output signal is depicted below each set of carriers..

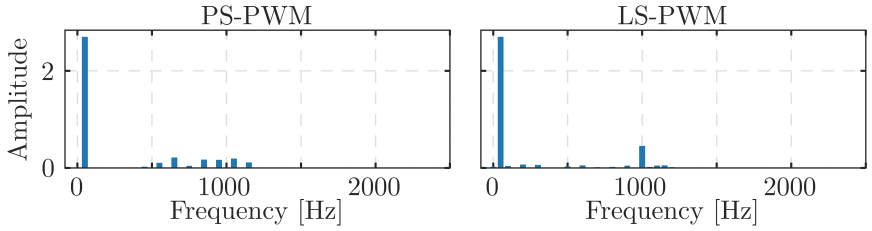

Figure 1.21 Magnitude spectrum of the output signal for Phase- (left) and PD Level-shift (right) PWM approaches shown in Fig. 1.20.

means phase a is connected to level 3, phase b to level 2, and phase c to level 4. There is no exact nomenclature for the levels, and the literature usually range them either using $[(-N+1)/2,(N-1)/2]$, $[1,N]$ or $[0,N-1]$. Nevertheless, this section will denote the levels from 1, being the negative side of the dc-link or the lowest level of voltage, to N being the positive side of the dc-link or the largest level of voltage. In any case, depending on what the reference for measuring the output voltage v_i is, the duty ratio obtention of the switching vector has to be defined accordingly.

Given that multilevel converters have more switching positions, the space vector region is no longer composed of 6 regions as previously shown in Fig. 1.6. Instead, the space vector region, seen as the $\alpha\beta$ plane, incorporates as many inner hexagons as additional levels in such a way that all switching states are represented and evenly spaced. Again, this disposition comes from positioning each switching vector in the abc space, and then rotating the view such that it lies perpendicular to the $\alpha\beta$ plane, so the common component is obviated. Due to the latter, the switching vectors that only differ in the common component, i.e. that yield the same phase-to-phase voltage, are made explicit as

they lie superposed on the same point. These switching vectors are referred as redundant ones, and thus they can be considered in the output voltage vector modulation as the same one. However, they are specially relevant for capacitor voltage balancing tasks, as it will be mentioned later.

Again, the modulation process consists in selecting and sequencing the switching vectors along a switching period to replicate the desired output voltage $x_{\alpha\beta}$. This is achieved by means of computing the duty ratios of each of the involved switching vectors. Using M switching vectors, the following constraints have to be fulfilled

$$1 = \sum_{m=1}^{M} d_m \tag{1.71}$$

$$x_\alpha = [d_1 \dots d_M] \begin{bmatrix} [a_1 b_1 c_1] T^T_{abc\to\alpha} \\ \vdots \\ [a_M b_M c_M] T^T_{abc\to\alpha} \end{bmatrix}; x_\beta = [d_1 \dots d_M] \begin{bmatrix} [a_1 b_1 c_1] T^T_{abc\to\beta} \\ \vdots \\ [a_M b_M c_M] T^T_{abc\to\beta} \end{bmatrix}, \tag{1.72}$$

where $n = 1, \dots, N$ is the index of the N used switching vectors, and $[a_n\, b_n\, c_n]$ is the corresponding levels in the considered n switching vector. With this formulation, any number of switching vectors (M) can be utilized as long as the duty ratio constraints are fulfilled.

Once the switching positions are selected and their duty ratios are computed, the sequencing and the redundant switching vector selection have to be carried out. Indeed, this process is not straightforward, and its proper design can achieve reduced losses, reduced distortion or elimination of common-modes in the output [30]. Every switching vector has a particular effect on the capacitor voltage balancing according to the levels it involves, and thus their selection determines how the voltage balancing is achieved. As it was mentioned previously, the redundant switching vectors achieve the same phase-to-phase output voltage but connect the output to different levels, and therefore the dc-link capacitors are charged/discharged differently. For example, consider switching vector '221' and its redundant one in a three-level converter '332'. The first vector involves levels 2 and 1, whereas the second one involves levels 3 and 2. This means that the first vector will inject/subtract current to/from levels 2 and 1, while the second one will do so to/from the levels 3 and 2. Some SVM strategies base its capacitor voltage balancing in this fact without affecting the modulated output voltage. However, it is worth mentioning that the largest the module of the switching vector, i.e. those that are in the outer limits of the SV hexagon, have no redundant vectors, so the redundant switching vector strategy alone might not be enough to guarantee proper capacitor voltage balancing under some operating conditions [75]. For this, some strategies avoid using the three nearest switching vectors and aim at using more distant ones that have more redundant vectors available, and thus the capacitors can be properly balanced [76]. Alternatively, there exists the concept of virtual space-vector that is based on positioning additional switching vectors—called virtual vectors—that are a combination of other existing vectors, and thus their balancing capabilities can be taken into account [77, 78].

In any case, as the amount of levels increases so does the complexity of the SVM as there are more switching vectors and more capacitors to balance. For this, several strategies have been developed to reduce the computational burden of this approach when used with more than three-level topologies [79, 80]. To depict this, Fig. 1.22 shows the SVM hexagon for different levels where each point represents a switching vector—and its inherent redundant ones, where each step towards the centre adds one redundant position. Despite the fact that it is more common to find odd multilevel converters—due to the grid code limits for odd harmonics being higher than the even ones—, there exists multilevel converters with even number of levels.

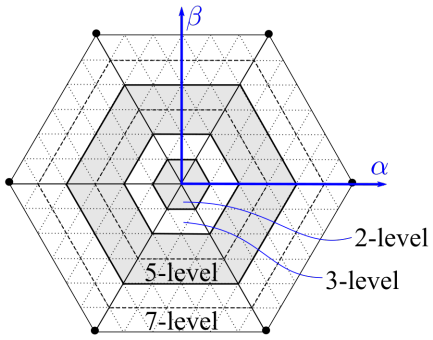

Figure 1.22 Multilevel space vector hexagon for different levels. Each crossing point represents one switching position.

In spite of considering SVM and carrier-based PWM different modulations, there are several studies that proved that they are different ways of facing the same problematic. Indeed, it is shown that for a particular configuration of the carriers and the injection of a common component in the modulated voltage for CB-PWM, the phase-to-phase output voltage waveforms matches those of SVM [81]. Nevertheless, the SVM makes more explicit the possible alternatives when modulating a three-phase output voltage as there are infinite possibilities of sequencing the switching vectors—by spreading them along the period, changing the sequence order, weighting among different redundant vectors, etc. Obviously, by defining particular objectives—such as reduced output distortion, reduced common-mode, reduced switching losses—the sequencing is selected accordingly [82].

Optimal PWM Schemes

This subsection exhibits that the modulations previously referred as Optimal PWM schemes (SHE) can be also used for multilevel converters. For this, the switching angle computation has to consider different level steps, which usually are sequenced consecutively in order to reduce the output voltage distortion [83]. Note that, for the two-level implementation, the switching angles are usually computed offline and stored in a look-up table (LUT), that is later used in online operation using the modulation index and the grid angle as inputs. Therefore, when the capacitor voltage balance task of multilevel converters have to be taken into account, a different LUT might need to be used instead depending on the balancing approach considered.

Work [84] carries out a comprehensive review of different balancing approaches to be used for SHE. Initially, three stages in the SHE approach are clearly stated: Switching angle acquisition, where the LUT is called and the switching positions are determined; waveform generation, where the output waveform is constructed based on the previous switching angles; and optimal state selection, that selects the more appropriate switching vector according to the cost function defined. Furthermore, it differentiates eight balancing methods: self-balancing control, charge amount regulation, zero-sequence harmonic adjustment, redundant switching angle sets adjustment, angle modification, selective harmonic elimination model predictive control, space voltage vectors adjustment, and redundant states adjustment. The main difference between these balancing approaches lies in the stage where they take place and the variables they modify. If they take place in the first stage, the LUT is usually modified such that the switching angles take the balancing task into account. If they take place in the second stage, the switching angles are slightly modified according to the capacitor voltages and current measurements in order to deal with the balancing. In contrast, if they take place in the third stage, the voltage waveform has been already defined as the output voltage reference and the most suitable switching vector is selected such that it also takes the balancing into account—which is equivalent of using the redundant vector strategy.

Nevertheless, finding a generalized and well-performing voltage balance approach for multilevel converters is a challenging task, given the noticeable differences that exist between multilevel topologies. Therefore, the most suitable balancing approach within SHE highly depends on the system topology and it has to be selected according to the target application.

1.3.3 Control without modulation

This section exposes some controllers that do not have a modulation stage, i.e. the gating signals of the switching devices are directly generated from the output of the controller. Usually, the controller is designed to select the switching position that yields the lower value of a cost function, or reduce as much as possible a tracking error. In general terms, these controllers achieve faster transient operation at the cost of a more spread harmonic spectrum, in other words, the output frequency spectrum is not centered around particular frequencies—the switching frequency for CB-PWM, for example—but a random distribution is obtained instead. This is mainly due to the fact that the controller does not modify the switching position at a fixed rate, but instead selects the position that achieves the best performance according to the law formulation. For the case of multilevel converters, the voltage balance task is covered by considering how the capacitor voltages may diverge into the state variables that composes the tracking error or the cost function. In the following, some of the most well-known approaches that can be considered inside this category are explained.

Hysteresis Control

This strategy was originally implemented using analog controllers where the real magnitudes are sampled continuously, although there exists digital implementations nowadays. The most well-known approach is the hysteresis current control, where a hysteresis band is

defined around each current tracking error and the switching output of the corresponding phase is changed whenever it crosses this band. Due to this, it requires continuous sampling in order to keep the current error within the band boundaries. However, a digital implementation would not allow a change in the switching action until the next sampling instant, and thus the tracking error of digitally-implemented hysteresis controllers will usually exceed the given boundaries.

In the case of multilevel converters, there exists several approaches that arrange the bands differently. Nevertheless, they share the same principle, the use of several bands with different widths around the tracking error—known as the multiband strategy—in such a way that the output level consecutively increments or decrements whenever the tracking error crosses them. Paper [85] presents a compilation of these approaches and exhibits their main benefits and drawbacks. Note that this approach alone does not consider the capacitor voltage balance, and thus an external agent, either by software or hardware, is required.

Direct Torque/Power control (DTC/DPC)

Similarly to the previous control, the direct torque/power control tracks the torque/power references using hysteresis controllers and a LUT to select the most suitable switching vector according to the current state of the system. Direct torque control was proposed first and it is well-established in the industry due to its simple control structure, fast response and robust operation. Direct power control was proposed afterwards for grid-connected converters to track the active and reactive power directly. Both controllers use the same principle but for the tracked variables and the LUT generation. Obviously, the LUT generation is carried out offline and depends on the system topology.

In terms of multilevel converters, the concept remains the same but the LUT generation have to consider all available switching vectors. Note that the principle of using redundant switching vectors for capacitor voltage balance can be applied in this approach [86]. Therefore, once the switching vector position is obtained from the LUT according to the variable tracking error, the more convenient vector among the redundant options can be selected.

Alternatively, some approaches avoid the use of LUTs and implements other controllers instead to achieve the same goal. Despite the fact that they usually require a modulator, they have been mentioned in this subsection as they share the same objective than DTC/DPC. This is the case of [87], where a controller gives the optimum output voltage vector that is modulated either using the nearest switching state or through SVM. Similarly, paper [38] develops a model-based direct power control where linear controllers are applied to obtain the optimum output voltage vector that is modulated through SVM or CB-PWM. Again, redundant switching vectors can be used to achieve capacitor voltage balancing in both approaches.

Finite-control-set model predictive controller (FCS-MPC)

This approach is one of the controllers that is leading the trend in optimal nonlinear controllers due to the development and evolution of digital systems. They are based on

a cost function that assists on indicating the optimal behaviour, and selecting the best switching vector by predicting the system state using model-based equations. For this, the objectives of the controller, namely dc-link voltage regulation, current tracking, minimum switching losses and capacitor voltage balance, are included in the cost function and all available switching actions are pondered with it, resulting in one switching vector having the minimum value, which is selected as the optimal one. This process is carried out every switching period to update the most suitable switching vector, and thus the controller performance highly depends on the switching frequency. Note that any system constraint or control objective can be formulated in the cost function, which is an advantage over other approaches as different objectives might be pursued [88].

The prediction horizon can be extended up to k switching events, which results in a controller with better performance. In this way, every switching instant, the controller computes the more convenient sequence of switching actions for the next k switching events, and selects the first one as the output. This controller can be easily adapted to multilevel converters by considering all possible switching actions and including the capacitor voltage balance objective inside the cost function [89]. Notice that some control objectives may be contradictory to each other, so it is necessary to tune weighting parameters to ponder the priority of such objectives.

This type of controllers are generally used to enhance the system performance over the whole operation range of the system, especially under transient conditions. As a downside, the computational burden of this approach is larger than those that use a modulation stage, specially for multilevel converters as the whole set of switching actions have to be evaluated using the cost function. Besides, the number of required computations exponentially increases with larger values of prediction horizon. For this, some works aim to reduce the computational burden by including some simplifications on the prediction stage or by avoiding the evaluation of some switching vectors when consecutive horizons are considered [90, 91].

Hybrid controllers

Despite the fact that the controllers exhibited in this section of control without modulation take into account the discrete nature of the system and avoid the use of averaged models, i.e. the use of duty ratios, the approaches inside the category of hybrid controllers explicitly consider the continuous nature of the state variables, i.e. the voltages and currents. Similarly to FCS-MPC, they directly consider the switching actions to control the converter, and therefore they do not require a modulator. The main differences with FCS-MPC is that an embedded control is proposed in the formulation of the hybrid dynamical systems. From the control perspective, the modelling is approached taking into account the hybrid nature of the system, and this framework allows, under some assumptions, to guarantee system stability.

Paper [92] implements this type of controller in a half-bridge inverter, where the desired output voltage—usually a sinusoidal waveform—is included in the system dynamics as an exogenous input generated by a time-invariant exosystem. From this, a hybrid dynamical system (HDS) with an embedded control law is considered, guaranteeing the existence

of a compact attractor where the tracking error—induced by the previous exogenous input—equals zero.

Work [93] presents a hybrid controller for NPC converters. In order to perform the stability analysis under balanced grid voltages, the nonlinear time-varying grid voltages in $\alpha\beta$ are modelled inside a polytope—using an circumscribed square whose vertices are the peak values—, which is later used along the nonlinear model to derive a polytopic system. With this approach, the time-varying aspect of the grid voltages can be expressed as a linear combination of constant terms, that facilitates the stability analysis in terms of Lyapunov theory. Then, an embedded control law is considered using the HDS theory and the uniform global asymptotic stability is guaranteed by means of analyzing the previous polytopic system.

2 Contributions to Diode-Clamped Converters

There are things done today in electrical science which would have been deemed unholy by the very man who discovered electricity, who would themselves not so long before been burned as wizards.

BRAM STOKER

This chapter will present the main contributions regarding diode-clamped converters (DCC). As it was mentioned in the introduction chapter, DCCs are a type of multilevel converters that uses power diodes to clamp the different levels in the output. The principle of the DCC scheme is derived from the two-level VSC, where, for each phase, there is an upper switching device that has a counterpart in the lower side. Thus, for the two-level VSC, one signal is used for controlling both switching devices, and the output is governed by this signal. The same idea can be extended for additional levels by adding a pair of switching devices and a pair of diodes with its corresponding signal. In this way, the output can be governed by considering the set of signals that switch on the upper devices corresponding to the desired level to be output. This idea is depicted in Fig. 2.1, where a generic scheme of one phase N-level DCC is shown. Note that $S_n^i = 1$ denotes a generic closed switching device with index n within phase $i = a$,b,c, whereas $S_n^i = 0$ refers to an open switching device. Following the same nomenclature shown in Fig. 2.1, in order to connect the output of phase i (v_i) to a certain level o_j for $j = 1,\ldots,N-1$, all switching devices S_n^i for $n = j,\ldots,N-1$ must be switched-on. The only exception to this rule is for the lowest voltage o_N that requires all S_n^i to be switched-off. Note that, as mentioned in the previous chapter, in an N-level DCC, there are $2(N-1)$ switching devices with antiparallel diodes and $2(N-2)$ power diodes connected as shown in Fig. 2.1.

In spite of the fact that it is possible to design a DCC with any number of levels, the industry and literature have focused on the three- and five-level topologies. As the

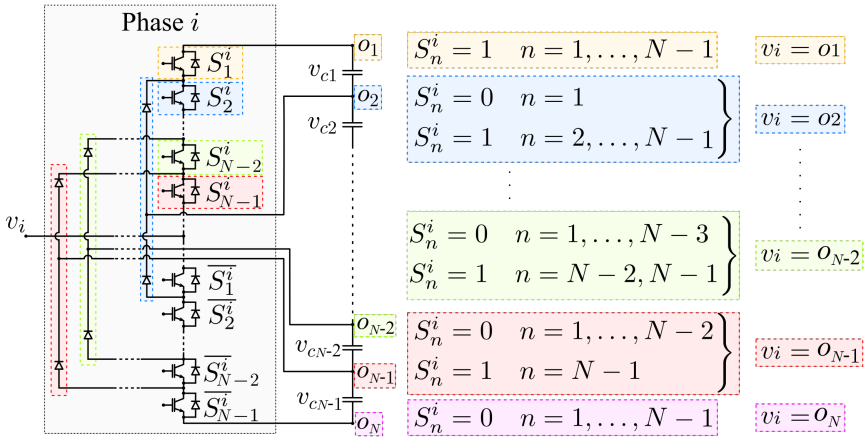

Figure 2.1 Scheme of one phase for a generic N-level DCC with possible switching combinations.

numbers of levels increases, so does the complexity on the converter control and the hardware requirements, and thus the incremental benefits of adding a level are degraded. In fact, every phase has N possible switching positions, where each of them connects the output phase to a certain level $j = 1,\ldots,N$ that affects the capacitor voltages below or above o_j depending on the phase current direction. Therefore, in a three-phase converter, there are N^3 possible switching positions and $N-1$ capacitors whose voltage has to be regulated. Due to this, the control complexity considerably increases with the number of levels, which explains the reluctance to use DCC with more than five levels. Besides, the switching device voltage limits goes from v_{dc}/N to $v_{dc}/(N+1)$ when an additional level is considered, and therefore this incremental benefit is downgraded as the number of levels increases. Nevertheless, the three-level topology is one of the most used and extended multilevel converter topologies for medium- and high-voltage applications [94], whereas the five-level topology can be found in some applications for motor drives [95, 96].

2.1 Principle of operation

As it is shown in Fig. 2.1, there are $N-1$ switching signals for $2(N-1)$ switching devices. In this way, the output v_i is connected to level o_j according to the switching signals as

$$v_i = o_j \text{ for } j \in [1, N-1] \quad \text{if} \quad S_n^i = 1 \ , n = j, j+1, \ldots, N-1 \tag{2.1}$$

$$v_i = o_N \quad \text{if} \quad S_n^i = 0 \ , n = 1, 2, \ldots, N-1. \tag{2.2}$$

Note that, for every switching position, the switched-on devices are next to each other, and thus, it is pointless to switch on a device that does not have, at least, another closed device next to it.

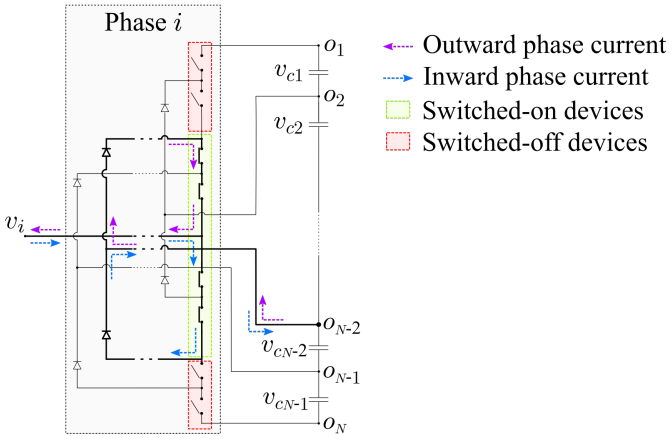

Figure 2.2 Example of inward and outward current path for a generic DCC with $v_i = o_{N-2}$.

The connection of phase i to the level o_j offers a path for the phase current, either inwards or outwards, by using both the switched-on devices and the power diodes. An example of such current paths for $v_i = o_{N-2}$ is shown in Fig. 2.2. Note that the open switching devices have to stand a voltage value of its corresponding capacitor thanks to the "clamping" effect of the power diodes. For example, considering the two lowest open switching devices in Fig. 2.2, they have to stand a total voltage of $v_{cN-1} + v_{cN-2}$, however a power diode clamps the middle point voltage in such a way that the lowest device have to support v_{cN-1} and v_{cN-2} the remaining one.

2.1.1 Switching states

Considering the scheme of Fig. 2.1, an integer variable called switching function $f_{ij} = 0,1$ can be defined in such a way that it expresses the current state of the converter [97]. This switching function equals 1 if phase i of the converter is connected to level o_j of the dc-link, and equals 0 otherwise. Considering that only one level can be output in any phase i, the constraint $\sum_{j=1}^{N} f_{ij} = 1$ has to be fulfilled for every phase i. In this way, the value of f_{ij} determines the switching signal values according to (2.1)–(2.2) given that $v_i = o_j$ means $f_{ij} = 1$ for $j = 1,\ldots,N$ and $i = a,b,c$. In Summary,

$$\left.\begin{array}{lll} f_{ij} = 1 & \text{if} & S_n^i = 1 \ , \ \forall n = j,\ldots,N-1 \ , \quad j = 1,\ldots,N-1 \\ f_{iN} = 1 & \text{if} & S_n^i = 0 \ , \ \forall n = 1,\ldots,N-1 \end{array}\right\} \tag{2.3}$$

$$\sum_{j=1}^{N} f_{ij} = 1. \tag{2.4}$$

Following this definition, the switching functions of Fig. 2.2 are $f_{iN-2} = 1$ and 0 for the remaining values of j.

As it was said in Chap. 1, it is common to use averaged models while dealing with power converters. This can be done considering that the switching functions are changed at much higher frequency than the controller bandwidth, and therefore the analysis can be still performed using averaged models. In this regard, the switching functions f_{ij} are averaged over a switching period in such a way that the duty ratio d_{ij} of each switching function is obtained. Considering this, the definition of duty ratio is the amount of time in a switching period that phase i is connected to level j, and thus, following the same constraint given in (2.4), $\sum_{j=1}^{N} d_{ij}$ must be fulfilled.

The above explanation of duty ratio and switching function can be used for other multilevel converter topologies, such as FC, by redefining (2.3) according to the topology layout.

2.1.2 Capacitor balancing

As it can be seen in the scheme given in Fig. 2.1, the current that inputs/outputs into each level o_j would flow through the dc-link capacitors, charging/discharging them accordingly. For example, in Fig. 2.2, an inward phase current would either charge v_{cN-2} and v_{cN-1} or discharge the remaining ones. In this regard, the current flow is determined by the switching position of the remaining phases, and therefore, for every set of three phase switching positions, there is a particular current path that would affect the charging/discharging of certain capacitors.

By using the duty ratios and considering the phase current i_i to be positive when it goes into the converter, the current that flows into a level o_j can be averaged as $i_{o_j} = \sum_{i=a,b,c} d_{ij} i_i$. Taking into account the capacitor voltage dynamics and the Kirchhoff equations on levels o_j, the following dynamic model can be formulated for every capacitor with capacitance C_n for $n = 1,\ldots,N-1$

$$\left.\begin{array}{ll} C_n \frac{d}{dt} v_{cn} & = i_{c_n} = i_{o_n} + i_{c_{n-1}} = \sum\limits_{i=a,b,c} d_{in} i_i + i_{c_{n-1}} \ , \ n = 2,\ldots,N-1] \\ C_1 \frac{d}{dt} v_{c1} & = i_{o_1} = \sum\limits_{i=a,b,c} d_{i1} i_i \end{array}\right\}, \quad (2.5)$$

where i_{c_n} refers to the the current flowing through capacitor C_n. According to (2.5), the charging of one capacitor depends on the current flowing through the capacitor that are placed above it. This fact manifests that the current path established by the switching positions of the three-phases together determines the charging/discharging of the capacitors. Fig. 2.3 depicts one example of current path for a particular three-phase switching position—phase a is connected to level $N-2$, phase b is connected to level 1, phase c is connected to level 2. Additionally, the switching vector that corresponds to the output voltage of the three phases measured from o_N is shown at the bottom. It is worth mentioning that the switching vector implements a normalization ($(N-1)/v_{dc}$) in order to refer to the voltage level of the phase output. Considering that a three-phase three-wire system has to fulfill $i_a + i_b + i_c = 0$, the currents flowing into node o_2 equal zero.

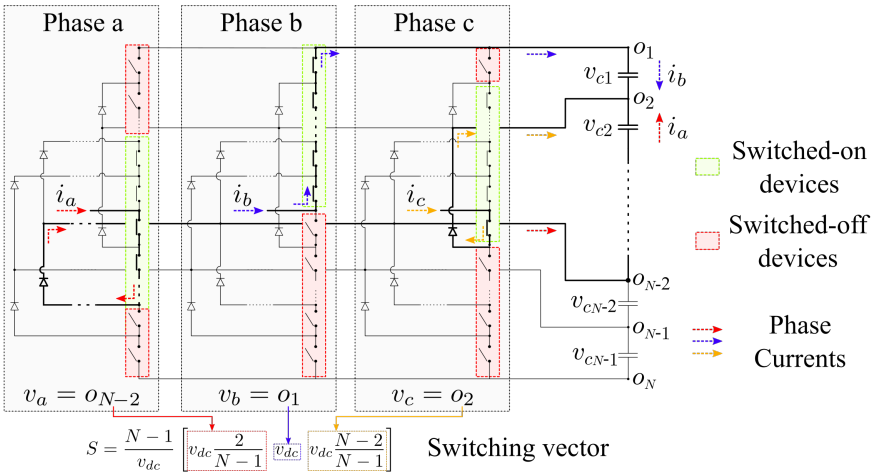

Figure 2.3 Example of current path set for a particular three-phase switching position, highlighting the affected capacitors.

Redundant switching vectors

As it was exposed in Chap. 1, in multilevel power converters, there exists the concept of redundant switching vectors. By representing all possible normalized output voltages of each phase in abc coordinates and translating them to the $\alpha\beta$ plane, the redundant switching vectors appear in the same position given that the homopolar component—γ component—is obviated in the $\alpha\beta$ representation. This means that the redundant switching vectors output the same normalized phase-to-phase voltage while using different levels. Indeed, this fact exposes one degree of freedom in the output voltage control that can be exploited to achieve capacitor voltage balancing.

In the $\alpha\beta$ representation—also referred as the SVM hexagon—the further the switching position is from the center, the lesser the amount of redundant switching vectors it has. In this regard, the zero vector—the center of the hexagon—has N redundant switching vectors, and every jump made to the immediate larger hexagon reduces the redundant switching vector by one. This is so until the outer hexagon is reached, where the switching positions have no redundant vectors—N jumps have been made. An example of three redundant switching vectors in a five-level DCC is shown in Fig. 2.4. Besides, the space vector region of a five-level DCC with the amount of redundant switching vector per inner hexagon is shown, where the switching vector example can also be seen. Note that the first vector [4 2 3] would modify the capacitor voltage of v_{c1} and v_{c2}, whereas vector [3 1 2] would do so for v_{c2} and v_{c3}, and vector [2 0 1] would do the same for v_{c3} and v_{c4}.

It is worth mentioning that the redundant switching vectors appear in the normalized representation of the output voltage vectors because equal capacitor voltages are assumed. When this is true, the jumps between levels are equal and they can be changed indistinctly. Looking at the example provided in Fig. 2.4, the phase-to-phase voltage between phase a and b (v_{ab}) are $v_{c1} + v_{c2}$, $v_{c2} + v_{c3}$ and $v_{c3} + v_{c4}$, respectively for each redundant vector. Therefore, the capacitor voltage values have to be equal to guarantee that the same phase-

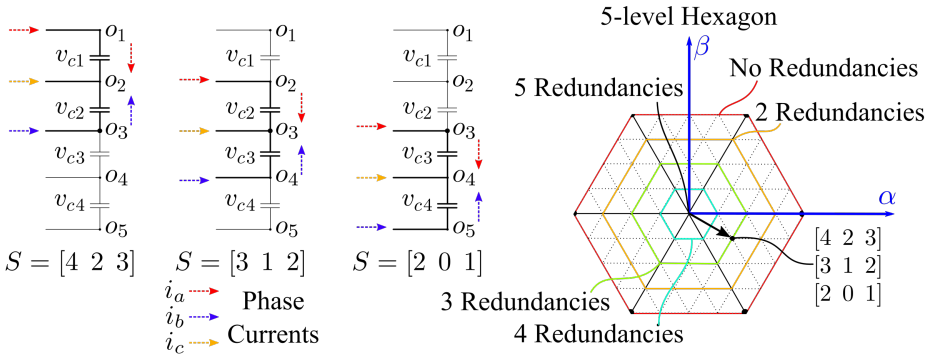

Figure 2.4 Example of three possible redundant switching vectors in a five-level DCC. Space vector region of a five-level DCC with the number of redundant switching vectors for each inner hexagon.

to-phase voltage is applied when selecting among redundant switching vectors. A work, presented later in this document, will expose this issue and it will propose a modulation approach that does not assume the capacitor voltages to be equal.

This concept of redundant switching vectors is also used in plenty of multilevel converter topologies, being one of the most used method to achieve capacitor voltage balancing.

In the following sections, the contributions made for three-level DCC and five-level DCC are exhibited along with the used modelling approach.

2.2 Three-level DCC: Neutral-point clamped (NPC)

This section is devoted to the grid-connected three-level topology of the DCC, which is also known as neutral-point clamped (NPC) converter. Several contributions for controlling and modulating grid-connected three-level NPC have already been presented that are not the aim of this work [60, 63].

The contribution for NPC exhibited in this work is focused on the hybrid modelling [92] of such a converter working as a rectifier in a grid-connected application [93]. This section presents some modifications of this latter work [93] that improves and allows its experimental validation [98]. Firstly, the main results of [93] in terms of modelling and control laws are introduced, then the developed modifications and experimental results are exhibited.

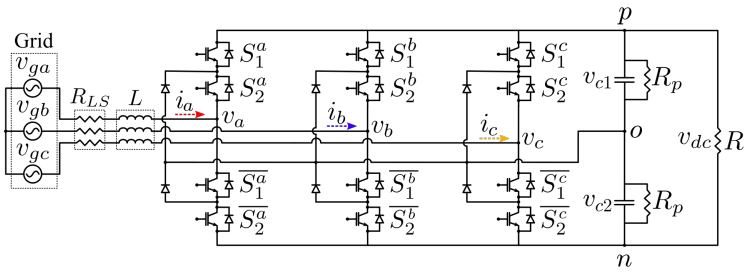

Figure 2.5 Scheme of grid-connected three-level NPC Converter.

2.2.1 System description

This subsection describes the converter scheme used to derive the modelling and the proposed control algorithm. The grid-connected NPC converter is shown in Fig. 2.5. The system is interfaced with the grid voltages v_{gi} for $i = a,b,c$ by means of an L-filter with same inductance L and parasitic resistance R_{LS}. The phase currents i_a,i_b and i_c are measured as positive when entering the converter—as depicted in Fig. 2.5. The dc-link is composed of two capacitors C_1 and C_2 with same capacitance C, whose capacitor voltages are v_{c1} and v_{c2} respectively, with an equalization resistor R_p attached in parallel to each of them. Lastly, to emulate some active power consumption, a resistive load R is attached to the dc-link side.

Dynamic Model

The NPC modelling formulated in [93] is derived and exhibited in this section. Considering Fig. 2.5 as reference, the model of the system dynamics can be formulated by applying Kirchhoff laws on the inductor and dc-link capacitors. In order to reflect the capacitor voltage unbalance between v_{c1} and v_{c2}, v_d is defined as

$$v_d \coloneqq v_{c1} - v_{c2}, \tag{2.6}$$

which allows to express each capacitor voltage as a function of the dc-link voltage and v_d as follows

$$v_{c1} = \frac{v_{dc}}{2} + \frac{v_d}{2} \tag{2.7}$$

$$v_{c2} = \frac{v_{dc}}{2} - \frac{v_d}{2}, \tag{2.8}$$

where $v_{dc} = v_{c1} + v_{c2}$.

The switching functions defined in (2.3) are used to model the possible switching position of each phase. To model this, the output voltage of each phase i (v_i), measured with respect to the dc-link neutral point o, is expressed according to the switching functions and (2.7)–(2.8) as follows

$$v_i = v_{c1} f_{ip} - v_{c2} f_{in}\,, \quad i = a,b,c \tag{2.9}$$

$$v_i = \frac{v_{dc}}{2}(f_{ip} - f_{in}) + \frac{v_d}{2}(f_{ip} + f_{in}), \quad i = a,b,c \tag{2.10}$$

where f_{ij} for $j = p,o,n$ is the switching function—this notation for the levels is adopted according to Fig. 2.5 for the NPC converter—, and $v_{dc} = v_{c1} + v_{c2}$. Using the inductor voltage drop equation, the model of the NPC phase currents can be stated as follows

$$L\frac{di_a}{dt} = v_{ga} - R_{LS}i_a - \frac{2}{3}v_a + \frac{1}{3}v_b + \frac{1}{3}v_c \tag{2.11}$$

$$L\frac{di_b}{dt} = v_{gb} - R_{LS}i_b - \frac{2}{3}v_b + \frac{1}{3}v_a + \frac{1}{3}v_c \tag{2.12}$$

$$L\frac{di_c}{dt} = v_{gc} - R_{LS}i_c - \frac{2}{3}v_c + \frac{1}{3}v_b + \frac{1}{3}v_a \tag{2.13}$$

where a balanced grid voltage $v_{ga} + v_{gb} + v_{gc} = 0$ is assumed. Besides, given that the converter is a three-phase three-wire system, the phase currents have to fulfill $i_a + i_b + i_c = 0$. Replacing (2.10) into (2.11)–(2.13)

$$\begin{aligned} L\frac{di_a}{dt} =& v_{ga} - R_{LS}i_a + \frac{v_{dc}}{6}(-2(f_{ap} - f_{an}) + (f_{bp} - f_{bn}) + (f_{cp} - f_{cn})) \\ &+ \frac{v_d}{6}(-2(f_{ap} + f_{an}) + (f_{bp} + f_{bn}) + (f_{cp} + f_{cn})) \end{aligned} \tag{2.14}$$

$$\begin{aligned} L\frac{di_b}{dt} =& v_{gb} - R_{LS}i_b + \frac{v_{dc}}{6}(-2(f_{bp} - f_{bn}) + (f_{ap} - f_{an}) + (f_{cp} - f_{cn})) \\ &+ \frac{v_d}{6}(-2(f_{bp} + f_{bn}) + (f_{ap} + f_{an}) + (f_{cp} + f_{cn})) \end{aligned} \tag{2.15}$$

$$\begin{aligned} L\frac{di_c}{dt} =& v_{gc} - R_{LS}i_c + \frac{v_{dc}}{6}(-2(f_{cp} - f_{cn}) + (f_{bp} - f_{bn}) + (f_{ap} - f_{an})) \\ &+ \frac{v_d}{6}(-2(f_{cp} + f_{cn}) + (f_{bp} + f_{bn}) + (f_{ap} + f_{an})). \end{aligned} \tag{2.16}$$

This dynamic model can be translated to the $\alpha\beta$ reference frame by applying the Clarke transformation (1.7), so the phase currents dynamics can be modelled with two equations

$$L\frac{di_\alpha}{dt} = v_{g\alpha} - R_{LS}i_\alpha - \frac{v_{dc}}{2}(f_{\alpha p} - f_{\alpha n}) - \frac{v_d}{2}(f_{\alpha p} + f_{\alpha n}) \tag{2.17}$$

$$L\frac{di_\beta}{dt} = v_{g\beta} - R_{LS}i_\beta - \frac{v_{dc}}{2}(f_{\beta p} - f_{\beta n}) - \frac{v_d}{2}(f_{\beta p} + f_{\beta n}) \tag{2.18}$$

The dynamic equations of the dc-link voltage and capacitor voltage error can be derived from the capacitor voltage equation

$$\begin{aligned} C\frac{dv_{dc}}{dt} = C\frac{dv_{c1}}{dt} + C\frac{dv_{c2}}{dt} &= \sum_{i=a,b,c} f_{ip}i_i - \frac{v_{dc}}{R} - \frac{v_{c1}}{R_p} - \sum_{i=a,b,c} f_{in}i_i - \frac{v_{dc}}{R} - \frac{v_{c2}}{R_p} \\ &= \sum_{i=a,b,c} (f_{ip} - f_{in})i_i - v_{dc}\left(\frac{2}{R} + \frac{1}{R_p}\right) \end{aligned} \tag{2.19}$$

$$C\frac{dv_d}{dt} = C\frac{dv_{c1}}{dt} - C\frac{dv_{c2}}{dt} = \sum_{i=a,b,c}(f_{ip}+f_{in})i_i - \frac{v_d}{R_p}, \tag{2.20}$$

which can also be translated to the $\alpha\beta$ reference frame, resulting in

$$C\frac{dv_{dc}}{dt} = \sum_{k=\alpha,\beta}(f_{kp}-f_{kn})i_k - v_{dc}\left(\frac{2}{R}+\frac{1}{R_p}\right) \tag{2.21}$$

$$C\frac{dv_d}{dt} = \sum_{k=\alpha,\beta}(f_{kp}+f_{kn})i_k - \frac{v_d}{R_p} \tag{2.22}$$

Note that phase current and capacitor voltage dynamics (2.21)–(2.22) use the switching function expressed in the $\alpha\beta$ reference frame. These variables are just the original switching functions f_{ij} for $i = a,b,c$ expressed in the $\alpha\beta$ plane using the Clarke transformation.

The previous equations can be transformed to obtain the dynamic model in terms of active (p) and reactive (q) powers. To do so, the instantaneous power theory is used as shown in Eq. (1.22). Using these expressions in model (2.17)–(2.18), the state-space model of the system can be obtained using variables p, q, v_{dc} and v_d as state variables

$$\underbrace{\begin{bmatrix}\dot{p}\\ \dot{q}\\ \dot{v_{dc}}\\ \dot{v_d}\end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} -\frac{R_{LS}}{L} & -2\pi f & -\frac{\xi_1}{2L} & -\frac{\xi_3}{2L} \\ 2\pi f & -\frac{R_{LS}}{L} & \frac{\xi_2}{2L} & \frac{\xi_4}{2L} \\ \frac{\xi_1}{CV_s^2} & -\frac{\xi_2}{CV_s^2} & -(\frac{2}{RC}+\frac{1}{R_pC}) & 0 \\ \frac{\xi_3}{CV_s^2} & -\frac{\xi_4}{CV_s^2} & 0 & -\frac{1}{R_pC} \end{bmatrix}}_{A_{u(m)}(t)} \underbrace{\begin{bmatrix}p\\ q\\ v_{dc}\\ v_d\end{bmatrix}}_{x} + \underbrace{\begin{bmatrix}\frac{V_s^2}{L}\\ 0\\ 0\\ 0\end{bmatrix}}_{B}, \tag{2.23}$$

where x refers to the state vector, $V_s = \sqrt{v_{g\alpha}^2 + v_{g\beta}^2}$ is the grid voltage amplitude, $f = \omega_g/(2\pi)$ is the grid frequency, and ξ_1, ξ_2, ξ_3 and ξ_4 are the variables related to the control inputs that are shown below. Note that terms $\pm 2\pi f$ appear due to the time derivative of the grid voltages given that a balanced three-phase grid voltage can be expressed as

$$v_{g\alpha}(t) = V_s\cos(2\pi f t) = \frac{dv_{g\beta}}{dt}\frac{1}{2\pi f}, \quad v_{g\beta}(t) = V_s\sin(2\pi f t) = -\frac{dv_{g\alpha}}{dt}\frac{1}{2\pi f},$$

and therefore, the state-space model derived in (2.23) assumes that the grid voltages are balanced.

Variables ξ_1, ξ_2, ξ_3 and ξ_4 are the input-related terms that depends on the switching vector position enumerated with the index m. In this way, the state matrix $A_{u(m)}(t)$ depends on the switching vector with index m considered. These variables are defined as follows

$$\xi_1 = u_1 v_{g\alpha}(t) + u_2 v_{g\beta}(t), \quad \xi_2 = u_1 v_{g\beta}(t) - u_2 v_{g\alpha}(t),$$
$$\xi_3 = u_3 v_{g\alpha}(t) + u_4 v_{g\beta}(t), \quad \xi_4 = u_3 v_{g\beta}(t) - u_4 v_{g\alpha}(t).$$

where $u^{(m)} = [u_1\ u_2\ u_3\ u_4]^T$ is the switching vector that is defined from the switching functions as

$$\begin{aligned} u_1 &= f_{\alpha p} - f_{\alpha n} \qquad & u_2 &= f_{\beta p} - f_{\beta n} \\ u_3 &= f_{\alpha p} + f_{\alpha n} \qquad & u_4 &= f_{\beta p} + f_{\beta n}. \end{aligned}$$

The previous expression can be rewritten in a matrix form as

$$\begin{bmatrix} \xi_1(t) \\ \xi_2(t) \\ \xi_3(t) \\ \xi_4(t) \end{bmatrix} = \begin{bmatrix} \Gamma(t) & 0 \\ 0 & \Gamma(t) \end{bmatrix} u^{(m)}\,, \quad \Gamma(t) = \begin{bmatrix} v_{g\alpha}(t) & v_{g\beta}(t) \\ v_{g\beta}(t) & -v_{g\alpha}(t) \end{bmatrix} \tag{2.24}$$

Note that the the state matrix $A_{u^{(m)}}(t)$ is time-dependant due to the fact that variables ξ_1,ξ_2,ξ_3 and ξ_4 depend on $v_{g\alpha}(t)$ and $v_{g\beta}(t)$. In this regard, let us recall the space vector region where all possible switching states, i.e. the finite number of control actions, are represented, which, for the NPC converter, are equal to $3^3 = 27$ positions. Thus, these positions can be numbered as $u^{(m)} \in U \coloneqq \{u^{(1)},\ldots,u^{(27)}\}$ according to the corresponding switching functions they represent. However, considering that the three zero switching states—positions $[nnn]$, $[ooo]$ and $[ppp]$—have no difference in the dynamics, two of them can be obviated on the set U, which is reformulated as $U \coloneqq \{u^{(1)},\ldots,u^{(25)}\}$.

2.2.2 Modelling of the grid voltages

As it was expressed above, the grid voltages are assumed to be balanced and sinusoidal. Thus, they represent a circumference in the $\alpha\beta$ plane whose radius is V_s as shown in Fig. 2.6. Taking advantage of this, they can be embedded into a polytope in the following way

$$\Omega \coloneqq \sum_{p=1}^{4} \nu_p \Omega_p\,, \quad \text{for} \quad 0 \le \nu_p \le 1 \ \text{ and } \ \sum_{p=1}^{4} \nu_p(t) = 1, \tag{2.25}$$

where Ω_p for $p = 1,2,3,4$ stands for the vertices of the polytope also shown in Fig. 2.6. The formulation of such vertices in the same $\alpha\beta$ plane can be given as follows

$$\Omega_1 = \begin{bmatrix} V_s \\ V_s \end{bmatrix}\,,\ \Omega_2 = \begin{bmatrix} -V_s \\ V_s \end{bmatrix}\,,\ \Omega_3 = \begin{bmatrix} V_s \\ -V_s \end{bmatrix}\,,\ \Omega_4 = \begin{bmatrix} -V_s \\ -V_s \end{bmatrix}.$$

In this way, the set that represents the grid voltages $\Phi = \{(v_{g\alpha}, v_{g\beta}) \in \mathbb{R}^2\,,\quad v_{g\alpha}^2 + v_{g\beta}^2 = V_s^2\}$ lies inside Ω.

Recalling $\Gamma(t)$ from (2.24), it can be rewritten as a linear combination of the four vertices that bound Ω as follows

$$\Gamma(t) = \sum_{p=1}^{4} \mu_p(t)\Gamma_p\,, \quad \sum_{p=1}^{4} \mu_p(t) = 1 \tag{2.26}$$

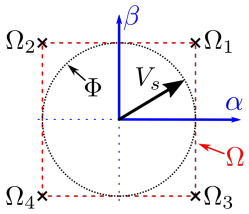

Figure 2.6 Grid voltage and polytope representation [93] in the $\alpha\beta$ plane.

$$\Gamma_1 = \begin{bmatrix} V_s & V_s \\ V_s & -V_s \end{bmatrix}, \Gamma_2 = \begin{bmatrix} -V_s & V_s \\ V_s & V_s \end{bmatrix}, \Gamma_3 = \begin{bmatrix} V_s & -V_s \\ -V_s & -V_s \end{bmatrix}, \Gamma_4 = \begin{bmatrix} -V_s & -V_s \\ -V_s & V_s \end{bmatrix},$$

which applied to the ξ definition in (2.24) results in

$$\begin{bmatrix} \xi_1(t) \\ \xi_2(t) \\ \xi_3(t) \\ \xi_4(t) \end{bmatrix} = \sum_{p=1}^{4} \mu_p(t) \begin{bmatrix} \Gamma_p & 0 \\ 0 & \Gamma_p \end{bmatrix} u^{(m)} \tag{2.27}$$

2.2.3 Polytopic system fomulation

According to (2.27), the state matrix $A_{u^{(m)}}(t)$, which depends on the ξ_p values, can also be written in a similar way

$$A_{u^{(m)}}(t) = \sum_{p=1}^{4} \mu_p(t) A_{u^{(m)}}(p), \tag{2.28}$$

where, for every instant of t, the time-dependant state matrix is represented as a linear combination of state matrices that are not time-dependant. State matrices $A_{u^{(m)}}(p)$ are the original state matrix but considering the fixed terms Γ_p in the definition of ξ_1, ξ_2, ξ_3, and ξ_4. Therefore, state matrix $A_{u^{(m)}}(p)$ can be expanded into matrices M_1, M_2, M_3, M_4 that multiply ξ_1, ξ_2, ξ_3, and ξ_4, respectively, and a common matrix M_0. Thus,

$$A_{u^{(m)}}(p) = \begin{bmatrix} M_1 & M_2 & M_3 & M_4 \end{bmatrix} \left(\begin{bmatrix} \Gamma_p & 0 \\ 0 & \Gamma_p \end{bmatrix} u^{(m)} \right) \otimes I_4 + M_0 \tag{2.29}$$

where $\otimes$ stands for the Kronecker product, and

$$M_0 = \begin{bmatrix} -\frac{R_{LS}}{L} & 2\pi f & 0 & 0 \\ -2\pi f & -\frac{R_{LS}}{L} & 0 & 0 \\ 0 & 0 & -(\frac{2}{RC} + \frac{1}{R_p C}) & 0 \\ 0 & 0 & 0 & -\frac{1}{R_p C} \end{bmatrix}$$

$$M_1 = \begin{bmatrix} 0 & 0 & -\frac{1}{2L} & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{CV_s^2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \; M_2 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{2L} & 0 \\ 0 & -\frac{1}{CV_s^2} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

$$M_3 = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{2L} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{CV_s^2} & 0 & 0 & 0 \end{bmatrix}, \; M_4 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{2L} \\ 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{CV_s^2} & 0 & 0 \end{bmatrix}.$$

Consequently, the nonlinear model exposed in (2.23) is expressed as a polytopic system [93]

$$\dot{x} = \sum_{p=1}^{4} \mu_p A_{u^{(m)}}(p) x + B \tag{2.30}$$

$$\Gamma(t) = \sum_{p=1}^{4} \mu_p(t) \Gamma_p \,, \quad \sum_{p=1}^{4} \mu_p(t) = 1$$

2.2.4 Control objectives

The main control objective is to make the state variables to converge towards their references, that is, $x \to x^*$. These references are given externally to this controller and they are defined as $[p^* q^* v_{dc}^* 0]$, where the reference for v_d is defined as zero to guarantee proper behaviour of the system.

Note that, while the state variables are continuous, the control signals, i.e. $u^{(m)} \in U$, are discrete. Thus, the proposed controller has to select the more appropriate switching action among the available ones in such a way that the previous objective is fulfilled. Another objective is to guarantee that the commutations do not occur at infinity frequency, that is, that a minimum dwell time occurs between consecutive commutations [99].

2.2.5 Proposed control law

For the control formulation, the hybrid dynamical system (HDS) theory is used, as it takes into consideration both the continuous and discrete nature of the system [100]. On the one hand, the continuous evolution (also called flow in HDS theory) comes from the state variable dynamics as it is expressed in the state-space model. On the other hand, the discrete evolution (also called jumps in HDS theory) is given when a change in the control input u happens.

In this way, the proposed control law can be embedded in the HDS formulation in the form $\mathcal{H} = (\mathcal{C}, f, \mathcal{D}, G)$ as

$$\mathcal{H} := \begin{cases} \begin{bmatrix} \dot{x} \\ \dot{u} \end{bmatrix} & = & f(x,u), & (x,u) \in \mathcal{C}, \\ \begin{bmatrix} x^+ \\ u^+ \end{bmatrix} & \in & G(x,u), & (x,u) \in \mathcal{D}, \end{cases} \tag{2.31a}$$

$$f(x,u) \coloneqq \begin{bmatrix} A_u(t)x+B \\ 0 \end{bmatrix},$$
$$G(x,u) \coloneqq \begin{bmatrix} x \\ \underset{u^{(m)}\in U}{\operatorname{argmin}}\ \tilde{x}^T P(A_{u^{(m)}}(t)x+B) \end{bmatrix}, \tag{2.31b}$$

$$\mathcal{C} :=\{(x,u) : \tilde{x}^T P(A_u(t)x+B) \leq -\eta\tilde{x}^T Q\tilde{x}\}, \tag{2.31c}$$
$$\mathcal{D} :=\{(x,u) : \tilde{x}^T P(A_u(t)x+B) > -\eta\tilde{x}^T Q\tilde{x}\}, \tag{2.31d}$$

where $\mathcal{C}$,$\mathcal{D}$ are the flow and jump sets, $\eta \in (0,1]$ is a design parameter, and matrices $P,Q \in \mathcal{S}^4$ are defined in such a way that they satisfy

$$A_{u^{(m)}}(p)^T P + P A_{u^{(m)}}(p) < -2Q\,, \quad p = 1,2,3,4\,, \quad u^{(m)} \in U. \tag{2.32}$$

In [93] it is proved that (2.32) can always be achieved by choosing P and Q using energy-like arguments.

The idea of (2.31) is based on the existence of a common Lyapunov function $V = \tilde{x}^T P\tilde{x}$ such that it decreases according to the selected $u^{(m)} \in U$. If the present control input $u^{(m)}$ gives a large enough decrement in V, then the same control input is kept, i.e. it flows according to set (2.31c). In the case it is not—set (2.31d)—, the control input is changed to the one that provides the lowest derivative of V as it is shown in $G(x,u)$ inside (2.31b).Note that parameter $\eta \in (0,1]$ can be tuned to adjust the number of jumps during transient time, i.e. the lower the η, the lower the number of jumps, and thus the lower frequencies the output voltage spectrum has.

It is worth mentioning that this controller do not use a modulator given that the switching function generation is implicit, similarly to FCS-MPC. Therefore, the output voltage spectrum would not be centered around a particular switching frequency as that of CB-PWM.

Summarizing, some features are required to guarantee that the Lyapunov function decreases enough after each jump, and that the hybrid system (2.31) is uniform global asymptotic stable (UGAS):

- For each $x \in \mathbb{R}^4$,

$$\min_{u^{(m)}\in U} \tilde{x}^T P(A_{u^{(m)}}(t)x+B) \leq -\tilde{x}^T Q\tilde{x}, \tag{2.33}$$

  has to be fulfilled.

- There exist a linear combination for the state matrix defined in (2.29) for $p = 1,2,3,4$ and $u^{(m)} \in U$ such that

$$\sum_{m=1}^{25}\sum_{p=1}^{4} \lambda_{m,p_{eq}} A_{u^{(m)}}(p)x_e + B = 0 \tag{2.34}$$

  holds, where $\lambda_{m,p_{eq}} \in [0,1]$ and $\sum_{m=1}^{25}\sum_{p=1}^{4}\lambda_{m,p_{eq}} = 1$.

- P and Q are positive definite.

Then, there exists an attractor set $\mathcal{A} := \{(x,u) : x = x^*, u \in U\}$ that is UGAS for the stated hybrid system [93]. The required proof for the above features and the attractor existence are also exhibited in [93].

In spite of the fact that a minimum dwell time is implicitly induced during transient behaviour ($\tilde{x} \neq 0$) by making Q strictly positive, the avoidance of a Zeno behaviour at steady-state is not guaranteed. For this, a modification in the hybrid system is performed that forces the solution to flow for a minimum time $T > 0$, which is equivalent to a minimum dwell time both for transient and steady-state conditions [99]. As a result, and similarly to the previous result, a compact set is established that is UGAS for the modified hybrid system

$$\mathcal{A}_T := \{(x,u,\tau) : \|\tilde{x}\| \leq X(T), u \in U, \tau \in [0, 2T]\}, \tag{2.35}$$

where T reflects the dwell time property, and set $\mathcal{A}_T$ can be arbitrarily close to $\mathcal{A}$ as long as T is small enough.

2.2.6 Experimental verification

This section exhibits the main contributions done to this approach, and it is devoted to the experimental validation of the above-mentioned controller. The motivation for the modifications introduced in the control law is to make the controller practically implementable and improve the steady-state performance,

Outer control loop

Considering the proposed embedded control law, the state variables references are given externally according to the desired equilibrum point (x^*). Theoretically, in steady-state conditions $\dot{x} = 0$, which dictates that the state variable references cannot be set arbitrarily. Indeed, this is obvious from the power flow perspective, where, in steady-state, the input flow of active power (the one given to the system from the grid) must match the output flow (the one absorbed by the load R in the dc side), otherwise the dc-link voltage would change inevitably. Despite the fact that this issue can be taken into account by making $\dot{x} = 0$ and defining x^* accordingly, in a real experiment there are additional losses, which are not considered in the model and that would make p^* to differ from the actual active power consumption at steady-state. Then, the previous controller cannot reach the steady-state in a real setup due to this mismatch.

For this, it is proposed to resort to the standard approach of VSC where an outer controller is used to set the active power reference p^* [101]. In this regard, a PI controller outputs the value of p^* from the quadratic error of the dc-link voltage ${v_{dc}^*}^2 - v_{dc}^2$ as the input. The tuning process of such controller can follow the standard approach exhibited in the introduction chapter, Sect. 1.2.4. The control parameters are denoted as $K_{p_{dc}}$ and $K_{i_{dc}}$.

In summary, reference p^* is no longer defined as a fixed value but it is given as the output of the PI controller, and thus it is not a design parameter.

Switching state selection

According to the proposed control method in [93], when the current switching state $u^{(m)}$ does not decrease the Lyapunov function below a certain value—which is directly proportional to the value of η—, the jump condition (2.31d) is fulfilled and function $G(x,u)$ is applied (2.31b). However, function $G(x,u)$ dictates that the next control action $u^{(m)}$ has to be searched within set $U \in \{u^{(1)}, u^{(2)}, \ldots, u^{(25)}\}$, taking the one that yield the minimum value of $\operatorname{argmin} \tilde{x}^T P(A_{u^{(m)}}(t)x + B)$, $u^{(m)} \in U$. However, this criterium will always select the control input that reduces the state variable error as much as possible, without taking into account the nature of multilevel converter. Large switching vectors—those that are in the outer boundary of the space vector hexagon ($u^{(m)}$ for $m = 20, \ldots, 25$)—have a more immediate effect on the state variables—they have larger values in the derivative of the Lyapunov function—, and thus they are more likely to be selected when a jump is given. In the case this phenomenon occurs frequently, the neutral level (point o) would not be used and the system would not exploit the benefits of multilevel converters. From a practical point of view, it would be more appropriate to apply any switching action that indeed used the neutral level and that achieved a decrement of the Lyapunov function, if such action existed.

The interest behind using the neutral point o lies in the phase current ripple, given that the use of the inner level smooths the phase current chattering, and thus the active and reactive power ones. This effect can be noticed in the state-space model (2.23) by realizing that those switching positions that have any $f_{io} \neq 0$ also have lower values of ξ_1, ξ_2, ξ_3 and ξ_4. Therefore, lower derivatives of the state variables are expected in comparison with other switching positions.

In summary, when a jump is given, a mechanism to prioritize the search of the switching action among the ones that use the neutral point o would improve the steady-state behaviour of the system. For this, a modified set $U' \in \{u^{(1)}, \ldots, u^{(19)}\}$ is defined in such a way that it only includes those switching actions with at least one $f_{io} \neq 0$. Then, whenever a jump is given, function $G(x,u)$ is modified to search u within U' first and, in the case it does not decrease the Lyapunov function enough, the whole set U is considered instead. This can be expressed as follows

$$G(x,u) = \begin{bmatrix} x \\ \underset{u^{(m)} \in U'}{\operatorname{argmin}} \ \tilde{x}^T P(A_{u^{(m)}}(t)x + B) \end{bmatrix} \quad \text{if } (x^+, u^+) \in \mathcal{C}$$

else

$$G(x,u) = \begin{bmatrix} x \\ \underset{u^{(m)} \in U}{\operatorname{argmin}} \ \tilde{x}^T P(A_{u^{(m)}}(t)x + B) \end{bmatrix}.$$

With this proposal, the UGAS property is not spoiled as the whole control input set is still available for the controller, while an improvement in the switching action selection stage is achieved.

Experimental setup

This hybrid modelling with embedded controller has been tested in a grid-connected NPC of 10 kVA using a data acquisition system with an on-board programmable FPGA. The grid-connected setup is shown in Fig. 2.7. The system and control parameters are listed in Table 2.1. Note that the state variables references $\{q^*, v_{dc}^*, v_d^*\}$ shown in Table 2.1 are for the desired steady-state conditions unless a change is explicitly given to test the behaviour. As it is stated previously, the reference for the state variable p^* is regulated through the PI controller. Along these experiments, variable q^* is not set to zero to emulate the rectifier application, even when the resistor load is unplugged, although the algorithm might work under zero reactive power conditions.

Table 2.1 NPC system and controller parameters.

Parameter	Value
Inductance parasitic resistance, R_{LS}	$0.01\ \Omega$
Load resistance, R	$120\ \Omega$
Equalization resistor, R_p	$4\ k\Omega$
Inductor, L	$2\ m$H
dc-link Capacitor, C	$9.9\ m$F
dc-link voltage reference, v_{dc}^*	650 V
dc-link voltage difference reference, v_d^*	0 V
Grid voltage amplitude in $\alpha\beta$, V_s	$220\sqrt{3}$ V
Grid frequency, f	50 Hz
Reactive power reference, q^*	-2 kVAr
Proportional dc-link PI controller, $K_{p_{dc}}$	0.05
Integral dc-link PI controller, $K_{i_{dc}}$	0.1

Implementation

Despite the fact that parameter η has been implemented as a tradeoff variable between performance and number of jumps, under real operation, the system variables are discrete and it benefits from having low sampling times. There are several reasons regarding the choice of the sampling frequency

- The sample time determines when the state variables are measured, which in theory are assumed to be continuous. Therefore, the lower the sample time is, the closer the real implementation to a continuous sampling is.
- The computation required to select the control action is also performed in a discrete way as there is a computational burden associated to this process that limits the maximum sampling frequency.
- As it was shown in Chap. 1, the higher the switching frequency, the more effective is the grid-filter in reducing the effective chattering. Consequently, given that this

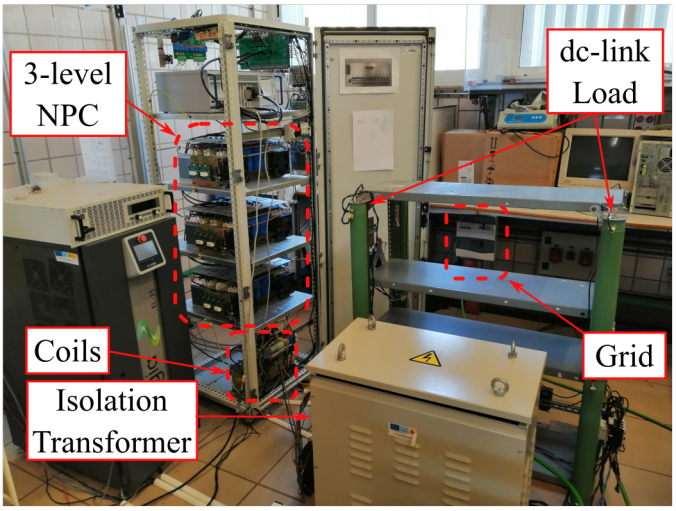

Figure 2.7 Experimental setup of the grid-connected NPC converter.

kind of controller do not center the output voltage spectrum around one frequency, lower sampling times potentially generate outputs with higher frequencies that are more easily filtered. Note that, for controllers that hold one control action between sampling instant, the switching frequency is equal or below the sampling frequency. Consequently, lower sampling times enable the system to achieve higher effective switching frequencies.

For this and considering the limitations in terms of overcurrents and equipment damage avoidance, the tests are performed with the largest sampling frequency achievable. For the experimental setup provided, this value is equal to a sampling frequency of 50 kHz, which is the maximum allowed considering the used Analog-to-Digital converters (ADC) and the computation time of the control. The latter implies to detect whether the system flows or jumps, i.e. computing set $\mathcal{C}$ (2.31c) and $\mathcal{D}$ (2.31d), and selecting the more appropriate switching action $u^{(m)}$ among the 25 available, which implies computing $\tilde{x}^T P(A_{u^{(m)}}(t)x+B)$ for every of them, in the case of a jump.

To achieve such a large sampling frequency, the algorithm must be implemented in the on-board FPGA of the data acquisition system. In this way, the sampling time is only limited by the ADC capture time and timing constraints of the FPGA mapping solution, which results in the above-mentioned 50 kHz. Notice that programming the FPGA requires the computations to be executed in fixed-point code, and therefore every variable has a predefined resolution and range.

The HDL Coder toolbox from *Matlab Simulink* along with several optimization options were used to develop the FPGA programming stage. Due to the nature of FPGAs, parallel computation is allowed as long as the FPGA resources allow for it, which facilitates reducing the computational time required for this approach. Firstly, $\tilde{x}^T P(A_{u^{(m)}}(t)x+B)$ is computed for every $u^{(m)}$; then, it is determined whether the system flows or jumps by considering the $u^{(m)}$ from the previous iteration and sets $\mathcal{C}$ and $\mathcal{D}$; lastly the new $u^{(m)}$

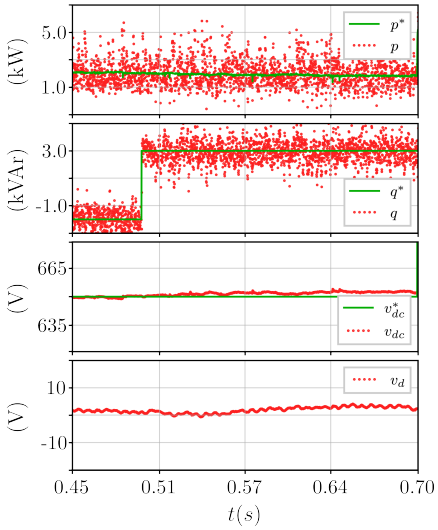

Figure 2.8 Experimental result: Change in the reactive power reference from $q^* = -2$ kVA to $q^* = 3$ kVAr with $\eta = 0.2$.

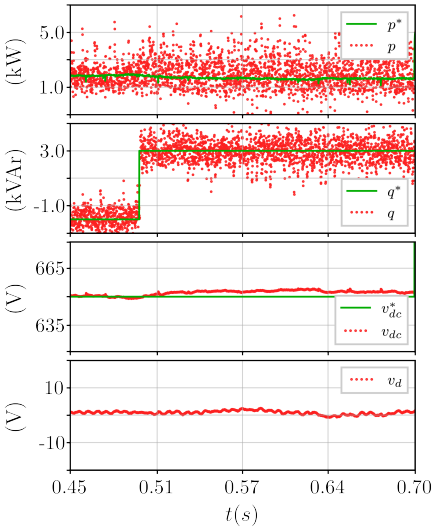

Figure 2.9 Experimental result: Change in the reactive power reference from $q^* = -2$ kVA to $q^* = 3$ kVAr with $\eta = 1$.

is selected, whether it is equal to the previous one (flow) or a new one (jump) that yields the lowest value of $\tilde{x}^T P(A_{u(m)}(t)x + B)$. Note that the modification of the switching state selection explained in the previous section is included in the last stage. At the end, the selected control input is decomposed into the gate signals for the switching of the semiconductor devices.

Matrices P and Q have to fulfill (2.32), and they have to be definite positive. For this, using linear matrix inequality (LMI) tools with the system parameters given in Table 2.1, the following P and Q matrices are obtained

$$P = \begin{bmatrix} 2.91 & 0 & 0 & 0 \\ 0 & 2.91 & 0 & 0 \\ 0 & 0 & 1.041 \times 10^6 & 0 \\ 0 & 0 & 0 & 1.046 \times 10^6 \end{bmatrix} \tag{2.36}$$

$$Q = \begin{bmatrix} 10 & 0 & 0 & 0 \\ 0 & 10 & 0 & 0 \\ 0 & 0 & 1 \times 10^{-7} & 0 \\ 0 & 0 & 0 & 5 \times 10^{-7} \end{bmatrix}, \tag{2.37}$$

which are used in the $\tilde{x}^T P(A_{u(m)}(t)x + B)$ computation.

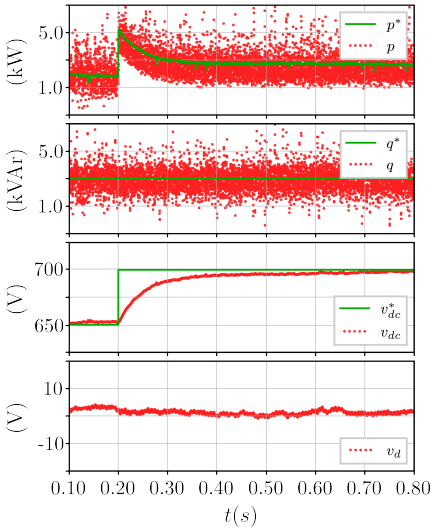

Figure 2.10 Experimental result: Change in the dc-link voltage reference from $v_{dc} = 650$ V to $v_{dc} = 700$ V with $\eta = 0.2$.

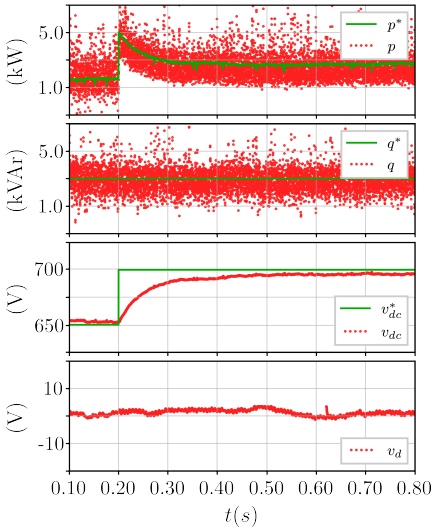

Figure 2.11 Experimental result: Change in the dc-link voltage reference from $v_{dc} = 650$ V to $v_{dc} = 700$ V with $\eta = 1$.

Experimental results

The experimental verification has been carried out through several tests. The system performance has been measured when a change in either q^* or v_{dc}^* is given, and when the load R is disconnected. Additionally, each of these tests have been carried out with $\eta = 0.2$ and $\eta = 1$. In the following, the state variables are represented through scatter plots, due to their sampled nature. The corresponding references are also depicted with them but for reference v_d^* which is zero, i.e. the balanced capacitor voltage condition is aimed.

- Figure 2.8 and 2.9 show the state variables evolution when a step in the reactive power reference is given from -2.0 kVAr to 3.0 kVAr at $t = 0.5$ s with $\eta = 0.2$ and $\eta = 1.0$ respectively.
- Figure 2.10 and 2.11 show the state variables evolution when a step in the dc-link voltage reference is given from 650 V to 700 V with $\eta = 0.2$ and $\eta = 1.0$ respectively. Again, the outer loop modifies the active power reference given that an increase in the dc-link voltage means an increase in the demanded dc-link load power.
- Figure 2.12 and 2.13 show the state variables evolution when the load is disconnected at $t = 0.2$ s with $\eta = 0.2$ and $\eta = 1.0$ respectively. Notice how the outer loop dictates the value of the active power reference in such a way that there is no mismatch between the active power and the power demanded from the load connected to the dc-link.

- Figure 2.16 and 2.17 show the state variables evolution when a disturbance of 20 V is given to v_d variable at $t = 0.2$ s with $\eta = 0.2$ and $\eta = 1.0$ respectively.

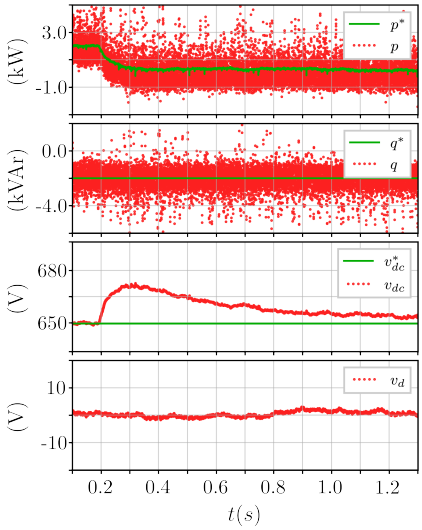

Figure 2.12 Experimental result: Disconnection of the dc-link resistor at $t = 0.2\,s$ with $\eta = 0.2$.

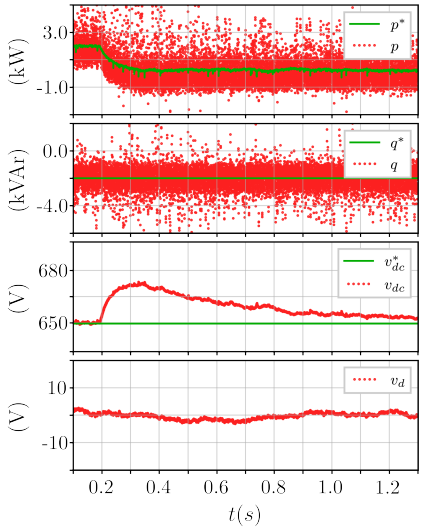

Figure 2.13 Experimental result: Disconnection of the dc-link resistor at $t = 0.2\,s$ with $\eta = 1$.

As it can be seen in Figs. 2.8 and 2.9, the reactive power dynamics are very fast, and thus the reference is tracked almost instantly. Alternatively, the dc-link voltage dynamic depends on the capacitor value and the outer loop time constant, and therefore tests in Figs. 2.10, 2.11, 2.12, and 2.13 take more time to reach steady-state condition. Nevertheless, the three tests depict no apparent differences in the behaviour between them when the value of η changes from $\eta = 0.2$ to $\eta = 1$, which can be explained due to the fast tracking of the active and reactive power and that the outer loop dynamic is not dependant on η. In contrast, Fig. 2.16 and 2.17 exhibits how the experiment with $\eta = 1$ achieves a faster regulation of v_d towards zero than the same experiment with $\eta = 0.2$. Indeed, this was one expected result as larger values of η make the control law more likely to select switching states that achieve faster regulation of the state variables. Fig. 2.14 depicts the three-phase currents at steady-state conditions with the parameters given in Table 2.1.

Figure 2.15 shows the switching index (m) that resulted from the algorithm when parameter η is equal to 0.2 and 1.0 during the v_{dc}^* change test. Considering that lower values of parameter $\eta \in (0,1]$ shrink set $\mathcal{D}$ according to (2.31d), it is easier to trigger a change of the current switching state for $\eta = 1$ than for $\eta = 0.2$. To validate this, the averaged numbers of commutations are measured during the v_{dc}^* change test (Fig. 2.10 and Fig. 2.11), resulting in

$$\eta = 0.2 \rightarrow 31.41 \ \frac{\text{comm.}}{\text{grid period}}$$

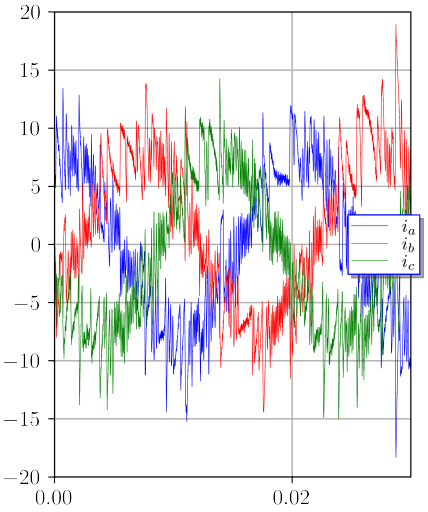

Figure 2.14 Three-phase currents at steady-state conditions with $q^* = -2$ kVAr, and the initial conditions given in Table 2.1.

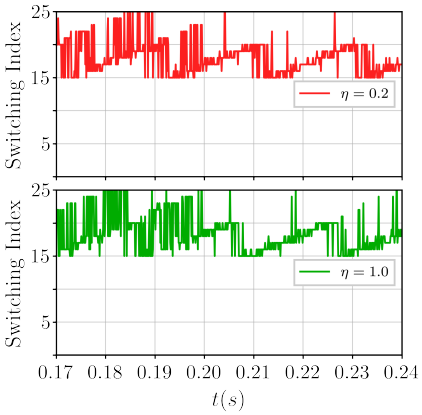

Figure 2.15 Selected switching index for $\eta = 0.2$ and $\eta = 1.0$ during the considered step in v_{dc}^* at $t = 0.2$ s.

$$\eta = 1.0 \rightarrow 35.98 \ \frac{\text{comm.}}{\text{grid period}},$$

which reflects that larger values of η indeed yield more commutations during transient operation.

2.2.7 Conclusions and future lines of research on NPC converters

The above analysis is focused on the development of a hybrid controller for the NPC converters, which has the advantage of not relying on an averaged model, and guaranteeing the existence of a desired attractor, which is proved to be UGAS. Additionally, parameter η can act as a tradeoff variable between the number of commutations and level of performance. The provided experiments along with the included modification with respect to [93] validate the approach.

Future lines of research include

1. Application of the proposed controller to other multilevel converters, whether they are of the same topology or a different one. This could be achieved by redefining the input-related terms—given that more switching functions could be derived—, and modifying the state matrix if required.

2. Use the polytopic model of the grid voltage to study the stability of other grid-connected power converters or microgrids. This method allows to overcome the difficulties a nonlinear grid voltage model introduces in the stability analysis of grid-related systems. Additionally, other geometries different from the square can be

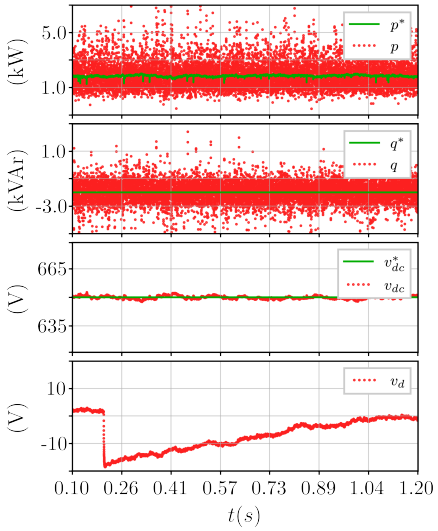

Figure 2.16 Experimental result: External disturbance of 20 V at $t = 0.2$ s in the v_d variable with $\eta = 0.2$.

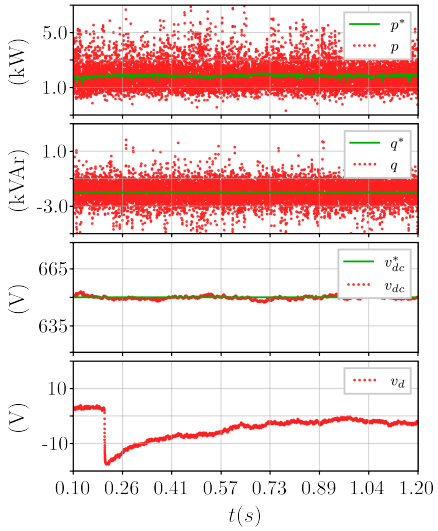

Figure 2.17 Experimental result: External disturbance of 20 V at $t = 0.2$ s in the v_d variable with $\eta = 1$.

applied for the polytope, such as an octogon, which could make the stability analysis less conservative and more affordable.

3. Include additional variables in the Lyapunov function or the state-space model in order to improve certain performance indicators, similarly to the model predictive control.

2.3 Five-level DCC

The schematic of a grid-connected five-level DCC is shown in Fig. 2.18. As it has been stated in previous sections, the use of five-level DCC is more uncommon compared to that of the NPC. This is due to its increased complexity in control and the increased hardware, which may outweigh the obtained benefits. Namely, the presence of several capacitors in the dc link, which requires additional control objectives to guarantee a proper voltage sharing among them, and the increased number of possible switching positions are what make the control design challenging for this kind of converter.

Regarding the capacitor voltage equalization, the literature uses several approaches that can be primarily divided into the following categories [102]:

1. Using redundant switching vectors along with modulation strategies and control schemes or injecting zero-sequence voltages in the modulation signals of carrier-based modulators.
2. Using additional circuitry.
3. Through external converters connected to the dc-link.

4. Applying predictive control strategies based on a discrete-time model.

5. Analyzing the capacitor voltage imbalance issue as a problem of regulating the multiple outputs of a nonlinear system subject to exogenous disturbances [103].

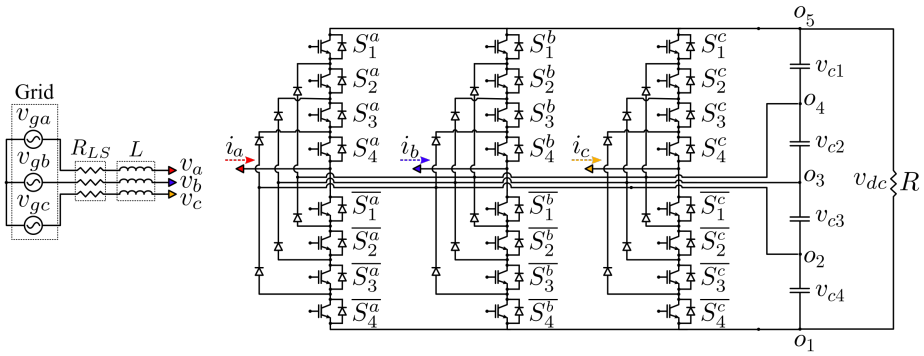

Figure 2.18 Scheme of grid-connected five-level DCC.

The first category will be explained at the end of this section as it requires a deeper explanation.

Some examples of the second approach are presented in [95, 104, 105]. However, given that they require additional hardware, they increase the converter cost and volume, and they do not guarantee that the control complexity is reduced or even kept the same. Despite these drawbacks, there are some upsides since the balancing task can be left to the external circuitry, and thus the five-level DCC can be exploited without this concern.

The third approach is limited to specific applications where the dc-link is attached to a source capable of regulating active power among the different levels, such as back-to-back converters [106] or active/passive front-ends [107]. Therefore, it is of no use when the dc-link is only composed of a passive element that is not connected to any other element.

The fourth approach covers predictive controllers, such as the current controller presented in [108], or the well known finite-control-set model-predictive control (FCS-MPC) [89]. However, these approaches usually require to compute some predictions for every possible switching action within the switching period, which in the case of 5-level DCC may be unaffordable. That is why great efforts are being devoted to come up with predictive controllers with reduced computational burden [109]. Note also that the control law exhibited in Sect. 2.2.5 for three-level NPC also relies on model-based computations to obtain the best switching action to select. However, in contrast to predictive controllers, it does not compute predictions but derivatives of the Lyapunov function candidate.

The last category is extracted from the proposal [103], where an integrated control and modulation is proposed. In summary, this proposal uses the averaged model to derive several control laws that dictates the behaviour of the modulation. This approach establishes the benchmark for several contributions of the present work, and thus it will be explained later in more detail.

Recalling the first category, it uses the redundant switching vectors or the injection of zero-sequence component [110, 111] to achieve balancing. As explained in subsection 2.1.2 for a n-level general case, this solution exploits the degree of freedom associated with the different switching combinations that achieve the same phase-to-phase converter voltage output. That is, making the phase current to circulate through different capacitors to regulate their own voltage without affecting the current performance. Indeed, given the usual $\alpha\beta$ transformation, this strategy is equivalent to the injection of zero-sequence component (γ component), as the redundant vectors appear superposed in the $\alpha\beta$ plane [112]. However, it has been stated that using the zero-sequence injection alone (or its equivalent redundant switching vectors in SVM) does not guarantee capacitor voltage balance when higher modulation indexes are given [113]. This is due to the lack of redundant switching vectors in the boundaries of the space vector region. To overcome this, [114] proposed to separate the space vector region into two regions according to the modulation index and a criteria for switching vector selection is provided. Alternatively, [115] uses the previous concept of duty ratios for each level which allows the control to consider all the degrees of freedom the converter has, that is, using several voltage levels within a switching period.

The research on this topology carried out by the author of this dissertation has resulted in five contributions, two of them published in field-related journals [116, 117], two published in conferences [118, 119], and one that is under review the moment this dissertation was being written [120].

2.3.1 System Description

This section uses the same nomenclature than the one used in the previous section, except for the additional switching devices, capacitors and levels. The dc-link is composed of four capacitors C_1, C_2, C_3 and C_4 with same capacitance C, whose capacitor voltages are v_{c1}, v_{c2}, v_{c3} and v_{c4}, respectively. For this topology and in contrast to the previous section, the dc-link equalization resistors and the line parasitic resistors are obviated given that the following proposed control schemes do not rely entirely on the circuit model. The five levels of the converter are numerated in ascending order according to its voltage level, i.e. from bottom to top, as o_j for $j = 1,\ldots,5$. Similarly to the NPC, the switching signals are numerated for each phase in descending order as S_p^i, and their counterpart as $\overline{S_p^i}$ for $i = a,b,c$ and $p = 1,\ldots,4$. Again, a resistive load R is attached to the dc-link side to emulate active power consumption.

2.3.2 Dynamic model

Considering the generic model of switching functions and duty ratios given in (2.1.1), the output voltage of the converter can be formulated in an averaged model ([97]) as

$$v_i = -(v_{c3}+v_{c4})d_{i1} - v_{c3}d_{i2} + v_{c2}d_{i4} + (v_{c2}+v_{c1})d_{i5}\,, \quad i = a,b,c. \tag{2.38}$$

Assuming that the capacitor voltage balance task is achieved in steady-state conditions, (2.38) can be further simplified by making $v_{c1} = v_{c2} = v_{c3} = v_{c4} = v_{dc}/4$, resulting in

$$v_i = \frac{v_{dc}}{4}(-2d_{i1} - d_{i2} + d_{i4} + 2d_{i5}) \,, \quad i = a,b,c \,, \tag{2.39}$$

or equivalently in the $\alpha\beta$ reference frame

$$v_k = \frac{v_{dc}}{4}(-2d_{k1} - d_{k2} + d_{k4} + 2d_{k5}) \,, \quad k = \alpha,\beta \,, \tag{2.40}$$

where the capacitor voltage unbalance has no effect given the previous assumption. From Fig. 2.18, the following model can be derived from the Kirchhoff laws and the inductor voltage drop

$$L\frac{di_a}{dt} = v_{ga} - \frac{2}{3}v_a + \frac{1}{3}v_b + \frac{1}{3}v_c \tag{2.41}$$

$$L\frac{di_b}{dt} = v_{gb} - \frac{2}{3}v_b + \frac{1}{3}v_a + \frac{1}{3}v_c \tag{2.42}$$

$$L\frac{di_c}{dt} = v_{gc} - \frac{2}{3}v_c + \frac{1}{3}v_b + \frac{1}{3}v_a \,, \tag{2.43}$$

which can be translated to the $\alpha\beta$ reference frame resulting in

$$L\frac{di_\alpha}{dt} = v_{g\alpha} - v_\alpha = v_{g\alpha} - \frac{v_{dc}}{4}(-2d_{\alpha1} - d_{\alpha2} + d_{\alpha4} + 2d_{\alpha5}) \tag{2.44}$$

$$L\frac{di_\beta}{dt} = v_{g\beta} - v_\beta = v_{g\beta} - \frac{v_{dc}}{4}(-2d_{\beta1} - d_{\beta2} + d_{\beta4} + 2d_{\beta5}) \,. \tag{2.45}$$

Following the same procedure and taking into account the DCC capacitor balancing generic formulation given in Sect. 2.1.2, the following averaged model for the capacitor voltages can be derived in $\alpha\beta$ reference frame

$$C\frac{dv_{c1}}{dt} = d_{\alpha5}i_\alpha + d_{\beta5}i_\beta - \frac{v_{dc}}{R} \tag{2.46}$$

$$C\frac{dv_{c2}}{dt} = (d_{\alpha5} + d_{\alpha4})i_\alpha + (d_{\beta5} + d_{\beta4})i_\beta - \frac{v_{dc}}{R} \tag{2.47}$$

$$C\frac{dv_{c3}}{dt} = -(d_{\alpha1} + d_{\alpha2})i_\alpha - (d_{\beta1} + d_{\beta2})i_\beta - \frac{v_{dc}}{R} \tag{2.48}$$

$$C\frac{dv_{c4}}{dt} = -d_{\alpha1}i_\alpha - d_{\beta1}i_\beta - \frac{v_{dc}}{R} \,. \tag{2.49}$$

It is worth mentioning that:

- The power invariant version of the Clarke transformation is the one being used to transform from abc to $\alpha\beta$
- The Clarke transformation includes the variables in the γ component. However, given that the system is a three-wire converter, the dynamics on this component can be neglected. Thank to this, there is an inherent degree of freedom in the reverse

transformation $\alpha\beta \rightarrow abc$ as the γ component can be selected arbitrarily. This feature is indeed related to the concept of using redundant switching vectors as it was mentioned before. Similarly, the obtention of the duty ratios in abc from those defined in $\alpha\beta$ can include such degree of freedom to address additional control objectives.

The capacitor voltage unbalance are represented through three variables v_{d1}, v_{d2}, v_{d3} defined as follows

$$v_{d1} = v_{c4} - v_{c1} \tag{2.50}$$
$$v_{d2} = v_{c3} - v_{c2} \tag{2.51}$$
$$v_{d3} = v_{c2} - v_{c1}\ . \tag{2.52}$$

By using (2.46)–(2.49), the dynamics of these variables can be obtained

$$C\frac{dv_{d1}}{dt} = -(d_{\alpha5} + d_{\alpha1})i_\alpha - (d_{\beta5} + d_{\beta1})i_\beta \tag{2.53}$$
$$C\frac{dv_{d2}}{dt} = -(d_{\alpha5} + d_{\alpha4} + d_{\alpha2} + d_{\alpha1})i_\alpha - (d_{\beta5} + d_{\beta4} + d_{\beta2} + d_{\beta1})i_\beta \tag{2.54}$$
$$C\frac{dv_{d3}}{dt} = d_{\alpha4}i_\alpha + d_{\beta4}i_\beta\ . \tag{2.55}$$

The dc-link voltage $v_{dc} = \sum_{p=1}^{4} v_{cp}$ dynamic is expressed from the addition of (2.46)–(2.49), resulting in

$$C\frac{dv_{dc}}{dt} = \frac{4}{v_{dc}}(v_\alpha i_\alpha + v_\beta i_\beta) - 4i_{dc}$$
$$C_{\text{eq}}v_{dc}\frac{dv_{dc}}{dt} = p - v_{dc}i_{dc}\ , \tag{2.56}$$

where $C_{\text{eq}} = C/4$ is the equivalent capacitance of the dc-link considering the four capacitors in series. As it can be seen, (2.56) represents the active power flow among the one obtained from the grid (p), the one used to increase the dc-link voltage ($C_{\text{eq}}v_{dc}\frac{dv_{dc}}{dt}$), and the one absorbed by the dc-link load ($v_{dc}i_{dc}$).

2.3.3 Integrated control and modulation of five-level DCC

This section exhibits the controller design presented in [97] and its further improvement and experimental validation [116], which are the contributions of this work. This controller reformulates the control inputs exhibited in (2.44)–(2.45) and (2.53)–(2.55) in such a way that the system control objectives are uncoupled and they can be targeted individually. Afterwards, the degrees of freedom related to the γ component are considered to further improve the system performance. In the following, the controller design, simulation results and experimental validation are exposed.

Controller design

Inspired from the current dynamic equations (2.44)–(2.45) and from the error signal dynamic equations (2.53)–(2.55), the following change of variables is carried out [97]

$$u_1 = -2d_{\alpha 1} - d_{\alpha 2} + d_{\alpha 4} + 2d_{\alpha 5} \tag{2.57}$$
$$u_2 = -2d_{\beta 1} - d_{\beta 2} + d_{\beta 4} + 2d_{\beta 5} \tag{2.58}$$
$$u_3 = d_{\alpha 5} + d_{\alpha 1} \tag{2.59}$$
$$u_4 = d_{\beta 5} + d_{\beta 1} \tag{2.60}$$
$$u_5 = d_{\alpha 5} + d_{\alpha 4} + d_{\alpha 2} + d_{\alpha 1} \tag{2.61}$$
$$u_6 = d_{\beta 5} + d_{\beta 4} + d_{\beta 2} + d_{\beta 1} \tag{2.62}$$
$$u_7 = -d_{\alpha 4} \tag{2.63}$$
$$u_8 = -d_{\beta 4}\,, \tag{2.64}$$

which can be synthesized in matrix form as follows

$$T_{k\to i} = \begin{bmatrix} 2 & 1 & -1 & -2 \\ 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 \\ 0 & -1 & 0 & 0 \end{bmatrix}$$
$$\begin{bmatrix} u_1 \\ u_3 \\ u_5 \\ u_7 \end{bmatrix} = T_{k\to i} \begin{bmatrix} d_{\alpha 5} \\ d_{\alpha 4} \\ d_{\alpha 2} \\ d_{\alpha 1} \end{bmatrix}; \quad \begin{bmatrix} u_2 \\ u_4 \\ u_6 \\ u_8 \end{bmatrix} = T_{k\to i} \begin{bmatrix} d_{\beta 5} \\ d_{\beta 4} \\ d_{\beta 2} \\ d_{\beta 1} \end{bmatrix}. \tag{2.65}$$

Therefore, the system dynamics result in the following equations

$$L\frac{di_\alpha}{dt} = v_{g\alpha} - \frac{v_{dc}}{4}u_1 \tag{2.66}$$
$$L\frac{di_\beta}{dt} = v_{g\beta} - \frac{v_{dc}}{4}u_2 \tag{2.67}$$
$$C\frac{dv_{d1}}{dt} = -u_3 i_\alpha - u_4 i_\beta \tag{2.68}$$
$$C\frac{dv_{d2}}{dt} = -u_5 i_\alpha - u_6 i_\beta \tag{2.69}$$
$$C\frac{dv_{d3}}{dt} = -u_7 i_\alpha - u_8 i_\beta \tag{2.70}$$

Therefore, u_1 and u_2 are the control inputs for the current controller for i_α and i_β, respectively, whereas u_m for $m = 3,\ldots,8$ can be used to formulate a capacitor voltage balancing controller that is independent from the current controller. Note, however, that it has been assumed equal capacitor voltage in the modelling stage, and thus, during transient periods where an unbalance is present, some distortions may appear in the current control loop.

Inner controller

Recalling the $\alpha\beta$ model in the stationary reference frame defined in Eq. (1.29) and comparing them with (2.66)–(2.67), it is straightforward that the control variables u_1 and u_2 can take the role of $4v_\alpha^*/v_{dc}$ and $4v_\beta^*/v_{dc}$, respectively, so any of the control strategies presented in the introduction can be used. In the remaining of this section, the model-based direct power controller presented in Sect. 1.2.4 is used (1.37)–(1.38), but with slight modifications in the formulation as follows

$$\begin{aligned} u_1 = u_1^{\text{eq}} &+ K_p v_{g\alpha}(p-p^*) + K_i v_{g\alpha}\int_o^t (p-p^*)d\tau \\ &- K_p v_{g\beta}(q-q^*) - K_i v_{g\beta}\int_o^t (q-q^*)d\tau \end{aligned} \tag{2.71}$$

$$\begin{aligned} u_2 = u_2^{\text{eq}} &+ K_p v_{g\beta}(p-p^*) + K_i v_{g\beta}\int_o^t (p-p^*)d\tau \\ &+ K_p v_{g\alpha}(q-q^*) + K_i v_{g\alpha}\int_o^t (q-q^*)d\tau\,, \end{aligned} \tag{2.72}$$

where a PI controller is used instead of a proportional one, so the integral gain compensates for model uncertainties. Consequently, the adaptation gain in (1.37)–(1.38) is no longer necessary—note that the adaptation gain was initially used to estimate the model uncertainties according to the actual measurements. In this way, the equilibrium point (1.38) is redefined

$$u_1^{\text{eq}} = \frac{4}{v_{dc}}\left(\left(1+\frac{\omega_g L q}{v_{g\alpha}^2+v_{g\beta}^2}\right)v_{g\alpha} + \frac{\omega_g L p}{v_{g\alpha}^2+v_{g\beta}^2}v_{g\beta}\right) \tag{2.73}$$

$$u_2^{\text{eq}} = \frac{4}{v_{dc}}\left(\left(1+\frac{\omega_g L q}{v_{g\alpha}^2+v_{g\beta}^2}\right)v_{g\beta} - \frac{\omega_g L p}{v_{g\alpha}^2+v_{g\beta}^2}v_{g\alpha}\right)\,. \tag{2.74}$$

Outer controller

Considering that a model-based direct power control is used for the IC, the OC should provide the power references p^* and q^* for it. In this work, considering the rectifier application of the converter (Fig. 2.18), a PI controller to regulate v_{dc} towards v_{dc}^* that provides the value of p^* is used, at the same time that q^* and v_{dc}^* are given externally by the user. The control parameters of this PI controller are named as K_p^{dc} for the proportional gain and K_i^{dc} for the integral gain.

Capacitor voltage controller

Lastly, the capacitor voltage balance controller, whose aim is to make the error signals v_{d1}, v_{d2}, v_{d3} to go to zero, can be derived from (2.68)–(2.70) as

$$u_3 = i_\alpha k_1 v_{d1}\,, \quad u_4 = i_\beta k_1 v_{d1} \tag{2.75}$$

$$u_5 = i_\alpha k_2 v_{d2}\,, \quad u_6 = i_\beta k_2 v_{d2} \tag{2.76}$$

$$u_7 = i_\alpha k_3 v_{d3}\,, \quad u_8 = i_\beta k_3 v_{d3}\,, \tag{2.77}$$

where $k_1 > 0$, $k_2 > 0$ and $k_3 > 0$ are the control parameters. With this formulation, (2.68)–(2.70) are transformed to

$$C\frac{dv_{d1}}{dt} = -k_1(i_\alpha^2 + i_\beta^2)v_{d1} = -k_1 I^2 v_{d1} \tag{2.78}$$

$$C\frac{dv_{d2}}{dt} = -k_2(i_\alpha^2 + i_\beta^2)v_{d2} = -k_2 I^2 v_{d2} \tag{2.79}$$

$$C\frac{dv_{d3}}{dt} = -k_3(i_\alpha^2 + i_\beta^2)v_{d3} = -k_3 I^2 v_{d3}\,, \tag{2.80}$$

where $I = \sqrt{i_\alpha^2 + i_\beta^2} \geq 0$ is the instantaneous amplitude of the currents when they are balanced. Nevertheless, given that k_1,k_2,$k_3 > 0$ and $I > 0$, it is straightforward that variables v_{d1}, v_{d2}, v_{d3} tend to zero.

Implementation

From the previous sections, the control inputs $u_1, \ldots, u_8$ are determined every switching period according to the implemented controller. Then, in order to feed the modulation stage, the duty ratios in abc are required. For this, firstly, the transformation shown in (2.65) is reversed to obtain the $\alpha\beta$ values of the duty ratios, then the four degrees of freedom $d_{\gamma 1}, d_{\gamma 2}, d_{\gamma 4}, d_{\gamma 5}$ are defined, and, lastly, the reverse Clarke transformation is carried out. Accordingly, the reverse of (2.65) is applied

$$T_{k\to i}^{-1} = T_{i\to k} = \begin{bmatrix} \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{2}{4} \\ 0 & 0 & 0 & -1 \\ 0 & -1 & 1 & 1 \\ -\frac{1}{4} & \frac{3}{4} & -\frac{1}{4} & -\frac{2}{4} \end{bmatrix}$$

$$\begin{bmatrix} d_{\alpha 5} \\ d_{\alpha 4} \\ d_{\alpha 2} \\ d_{\alpha 1} \end{bmatrix} = T_{i\to k} \begin{bmatrix} u_1 \\ u_3 \\ u_5 \\ u_7 \end{bmatrix} \tag{2.81}$$

$$\begin{bmatrix} d_{\beta 5} \\ d_{\beta 4} \\ d_{\beta 2} \\ d_{\beta 1} \end{bmatrix} = T_{i\to k} \begin{bmatrix} u_2 \\ u_4 \\ u_6 \\ u_8 \end{bmatrix}\,. \tag{2.82}$$

Afterwards, the values of $d_{\gamma j}$ for $j = 1,2,4,5$ can be determined aiming at additional control objectives. However, these values should not be selected arbitrarily as there exist several restrictions for the duty ratios in abc that may act as an upper and lower boundary for the value of $d_{\gamma j}$, that is, $\sum_{j=1}^{5} d_{ij} = 1$ and $d_{ij} \geq 0$ for $i = a,b,c$ should be fulfilled at all times. The original proposal [97] carried out some analysis based on the expected steady-state performance and proposed fixed values for these variables in such a way that duty ratio saturation is avoided. Consequently, $d_{\gamma j} = k_{\gamma j}$ for $j = 1,2,4,5$. As an alternative, variable $d_{\gamma j}$ values are considered in order to achieve an steady-state improvement which will be explained in the following subsection.

Once the previous steps have been carried out, the duty ratios can be obtained

$$\begin{bmatrix} d_{aj} \\ d_{bj} \\ d_{cj} \end{bmatrix} = T_{\alpha\beta\gamma\rightarrow abc} \begin{bmatrix} d_{\alpha j} \\ d_{\beta j} \\ d_{\gamma j} \end{bmatrix} \quad \text{for } j = 1,2,4,5\ , \tag{2.83}$$

and the duty ratio of the remaining level is derived from the duty ratio restriction

$$d_{i3} = 1 - \sum_{j=1,2,4,5} d_{ij} \quad \text{for } i = a,b,c\ . \tag{2.84}$$

With this, the duty ratios in abc are fully determined and the modulation stage can implement them along a switching period.

Algorithm Improvement

The four degrees of freedom, which correspond to $d_{\gamma j}$ for $j = 1,2,4,5$, are the homopolar component of each level for the three-phase set. They act as a bias for the four duty ratios simultaneously. Consequently, these values have three upper boundaries caused by the corresponding d_{i3} to reach zero—larger values of $d_{\gamma j}$ would make either $\sum_{j=1}^{5} d_{ij} > 1$ or $d_{i3} < 0$, which are both infeasible—, and one lower boundary for each level $j = 1,2,4,5$ that is reached whenever $d_{ij} = 0$ for any phase i—lower values of the corresponding $d_{\gamma j}$ would make, at least, one $d_{ij} < 0$. To take this into account, two solutions are proposed:

- Using fixed values $k_{\gamma j}$ for $j = 1,2,4,5$. This is the solution stated in the control proposal [97] and these values are derived from the expected steady-state behaviour in such a way that the maximum possible range of operation is allowed for the duty ratios. Note that, fixing $d_{\gamma j}$ would translate the upper and lower boundaries to the $d_{\alpha\beta j}$, which can be expressed as a delimited range for the control inputs $u_1, \ldots, u_8$.
- Using time-variant values in order to fully exploit the range of operation of the duty ratios, while some additional benefits are obtained. This is the case when the $d_{\gamma j}$ values are selected according to their lowest boundary, that is, when one $d_{ij} = 0$. Not only this keeps the remaining duty ratios the furthest possible from the upper bound, but also it avoids one level to appear in the output voltage, that is, at least one commutation is avoided. This is highlighted as a contribution of this work, and its benefits will be discussed and exhibited in the simulation and experimental section.

The second solution offers more benefits due to its flexibility, and thus it will be analyzed in the following.

The lower boundary for each $d_{\gamma j}$ comes from the reverse Clarke transformation (2.83), which results in three possible values,

$$d^a_{\gamma j} = -T_{\alpha\beta\rightarrow a} \begin{bmatrix} d_{\alpha j} \\ d_{\beta j} \end{bmatrix} = -\sqrt{2} d_{\alpha j} \tag{2.85}$$

$$d^b_{\gamma j} = -T_{\alpha\beta\rightarrow b} \begin{bmatrix} d_{\alpha j} \\ d_{\beta j} \end{bmatrix} = \frac{d_{\alpha j}}{\sqrt{2}} - d_{\beta j}\sqrt{\frac{3}{2}} \tag{2.86}$$

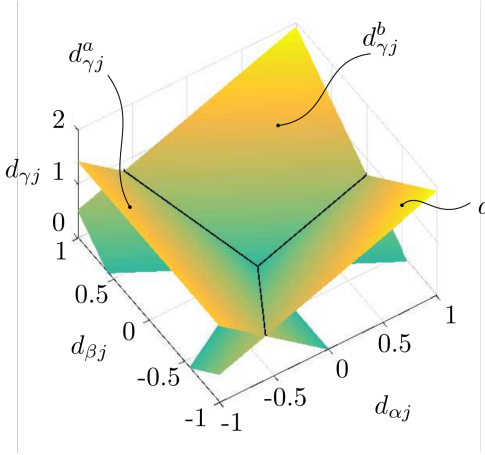

Figure 2.19 The planes represented by eqs. (2.85)–(2.87) in the $\alpha\beta\gamma$ region.

$$d^c_{\gamma j} = -T_{\alpha\beta\to c}\begin{bmatrix} d_{\alpha j} \\ d_{\beta j} \end{bmatrix} = \frac{d_{\alpha j}}{\sqrt{2}} + d_{\beta j}\sqrt{\frac{3}{2}}\,, \tag{2.87}$$

where $d^i_{\gamma j}$ stands for the value of $d_{\gamma j}$ that makes the corresponding duty ratio d_{ij} of phase i equal to zero. Considering this, and the constraint of $d_{ij} \geq 0$, the lowest boundary of $d_{\gamma j}$ is

$$d_{\gamma j} = \max\left(d^a_{\gamma j}, d^b_{\gamma j}, d^c_{\gamma j}\right)\,, \tag{2.88}$$

where max stands for the maximum function. Note that, using (2.88) and given that it is the lowest boundary, if some d_{ij} results to be greater than 1, it would mean that duty ratio saturation was unavoidable—some d_{ij} is either lower than zero or larger than 1—, i.e. some control signal is out of boundaries. In these cases, it is recommended to prioritize the fulfillment of the inner controller—the power control carried out by defining u_1 and u_2—over the capacitor voltage balancing—carried out by $u_3,\ldots,u_8$—, given the slower dynamic of the capacitor voltages, and that the power control fulfillment is a more critical target. The easiest way to achieve this is by making all balancing control variables $u_3,\ldots,u_8$ equal to zero such that no effect on the capacitor voltage balancing is expected. Nevertheless, as it will be shown later in simulation and experiments, these cases are rare, and in the worst scenario, they would take place during some particular transient conditions.

At this point of the duty ratio obtention, the values $d_{\alpha j}$ and $d_{\beta j}$ for $j = 1,2,4,5$ are already defined, and thus applying (2.85)–(2.88) results in the values of $d_{\gamma j}$. To depict this, equations (2.85)–(2.87) are represented as planes in the $\alpha\beta\gamma$ space in Fig. 2.19. For any pair of $d_{\alpha j}$ and $d_{\beta j}$ values, there always exists one maximum value which dictates the selected value of $d_{\gamma j}$.

As a result of using this tuning algorithm, for levels $j = 1,2,4,5$, there would be one phase i whose $d_{ij} = 0$. However, levels $j = 2,4$ deserves special attention. This proposal,

in general, exploits the five-level converter such that all levels are used every switching period, that is, the output voltage of each phase is a staircase waveform that passes sequentially through every level in ascending and descending order—i.e. a symmetric staircase waveform. However, were this algorithm improvement to be used, it could result in having one inner level $d_{ij} = 0$ while the subsequent outer level $d_{ij} \neq 0$. This means that a jump between two nonconsecutive levels would take place. In general, this is not a desired event given that it entails the switching-off/on of two devices simultaneously, which may compromise the voltage limits of them given possible gating miss-matches and tail current effects. To avoid this, the selection of $d_{\gamma j} = d^i_{\gamma j}$ for $j = 2{,}4$ is limited only when $d_{\gamma j} = d^i_{\gamma j}$ for its immediate outer level $j = 1{,}5$ is also selected, respectively. On the whole, the following procedure is proposed for the $d_{\gamma 5}$ and $d_{\gamma 4}$ determination, which can be similarly applied to the determination of $d_{\gamma 1}$ and $d_{\gamma 2}$.

1. Firstly, $d_{\gamma 5}$ is determined from (2.88) with $j = 5$. Let us refer the phase whose duty ratio of level five is zero as i_1, i.e. $d_{i_1 5} = 0$.
2. Secondly, compute $d_{\gamma 4}$ from (2.88) with $j = 4$, and obtain which phase would make its corresponding duty ratio for level four equal to zero. Let us refer that phase as i_2.
3. Lastly, check whether $i_1 = i_2$. If so, then $d_{\gamma 4}$ is left as the previously computed value. Otherwise, the original proposal is used—$d_{\gamma 4} = k_{\gamma 4}$—, given that $d_{i_2 5} \neq 0$ and $d_{i_2 4} = 0$ is an undesired result.

In summary, the algorithm improvement would always make, at least, two duty ratios equal to zero, that is, one for each level five and one. Besides, under certain circumstances, up to two additional duty ratios can be zeroed thanks to this algorithm. To depict an example, Fig. 2.20 shows the resulting switching functions and output voltage of phase i when the original and the improved algorithm are used. For this particular case, $d_{\gamma 5} = d^i_{\gamma 5}$ and $d_{\gamma 4} = d^i_{\gamma 4}$.

Simulation and experimental verification

This subsection is devoted to validate the previous approach by means of simulation and experiments. The control and system parameters are shown in Table 2.2. The system uses a digital and analog control unit (DACU) that carries out the control computation every sampling period (equal to the switching period shown in Table 2.2), and set the switching functions for every phase as shown in Fig. 2.20. The experimental setup is shown in Fig. 2.21. The original algorithm uses variables $k_{\gamma j}$ for $j = 5{,}4{,}2{,}1$ to define the $d_{\gamma j}$ values, whereas the algorithm improvement, referred as the modified one, carries out the steps mentioned in the previous section.

Test A: Variable operating point

The first carried out test (Test A) goes through different conditions to validate the feasibility of the proposed approach for variable operating points. The parameters that are modified are shown in Table 2.3 with the time instant/interval at/during which the change takes place.

The three-phase currents in steady-state conditions for the experiments are shown in Fig. 2.22 for the original and modified algorithm with $R = 60\,\Omega$ and $v_{dc} = 800$ V. The improvement achieves a reduction in the chattering. This is due to the effect that using a

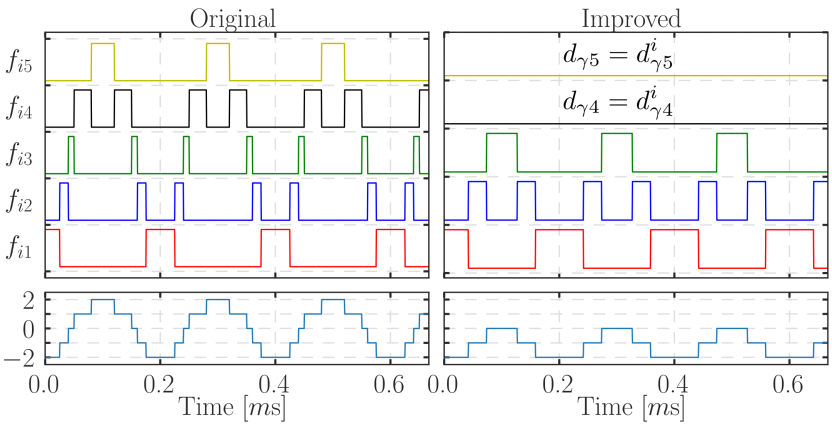

Figure 2.20 Sample of switching functions of phase i for the original and the improved algorithm (top), and the resulting output waveform (bottom). The improved algorithm shows the effect of having two duty ratios of two consecutive levels equal to zero. Switching frequency of 5 kHz.

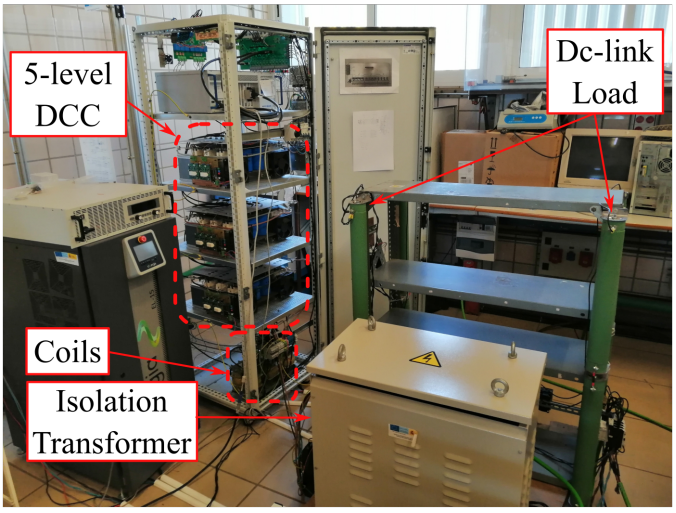

Figure 2.21 Experimental equipment of the five-level DCC.

reduced number of levels in the output voltage has. Despite the fact that the average model does not reflect differences between using different number of levels in the output, in reality, the phase currents exhibit chattering as a consequence of the modulation, i.e. a ripple at the switching frequency which depends on the levels used. Therefore, the modified algorithm not only reduces the switching losses by reducing the number of commutations, but also improves the steady-state performance. To further corroborate this, the harmonic

Table 2.2 Simulation and experimental parameters.

Parameter	Value	Parameter	Value
Switching freq., f_s	10 kHz	Grid freq., f_g	50 Hz
Grid Volt.	230 V_{RMS}	Filter Inductance, L	2 mH
dc-link capacitance, C	3.3 mF	Reactive. pow. ref., q^*	0 VAr
Cap. Volt. Bal., k_1,k_2,k_3	$5{\cdot}10^{-5}$	Prop. Pow. Con., K_p	$3{\cdot}10^{-7}$
Integ. Pow. Con., K_i	$5{\cdot}10^{-5}$	Prop. dc-link volt. Con., K_p^{dc}	0.05
Integ. dc-link volt. Con, K_i^{dc}	1	Fixed gamma val., $k_{\gamma 5}$,$k_{\gamma 1}$	0.7
Fixed gamma val., $k_{\gamma 4}$,$k_{\gamma 2}$	0.1		

Table 2.3 Parameters modified during test A.

Parameter	Init value	Final value	Time instant/interval
1. dc-link Resistor, R	120 Ω	60 Ω	0.7 s
2. dc-link volt. ref. v_{dc}^*	700 V	800 V	[2.6, 3.2] s
3. dc-link Resistor, R	60 Ω	120 Ω	4.7 s

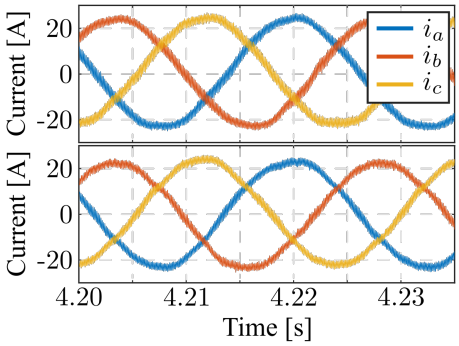

Figure 2.22 Experiment: Three-phase currents of proposed approach at steady-state for the proposed modulation (top) and the modified one (bottom). $R = 60\Omega$, and $v_{dc} = 800$ V.

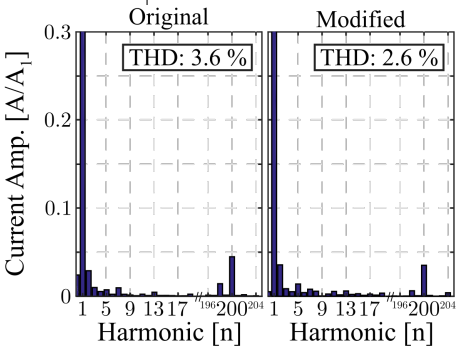

Figure 2.23 Experiment: Harmonic spectrum of phase a currents shown in Fig. 2.22 for the Original algorithm (left) and the modified one (right).

spectrum of these currents are shown in Fig. 2.23, where the total harmonic distortion (THD) of the original algorithm is 3.6 %, whereas the modified one yields a THD of 2.6%. As mentioned, the amplitude of the harmonic corresponding to the switching frequency ($n = 200$) is reduced with the modified algorithm.

To depict the effects the change in the parameters have on the system variables during experimental verification, Fig. 2.24 and Fig. 2.25 are depicted. Fig. 2.24 shows the v_{dc} variable and its reference v_{dc}^* during the changes considered in Table 2.3. This figure validates the outer controller performance as it regulates v_{dc} towards v_{dc}^*. As it can be seen, the changes in R act as external perturbations that are rapidly compensated, while

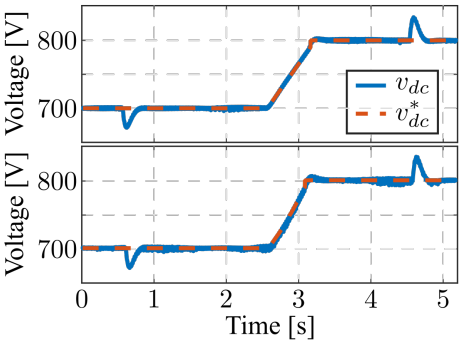

Figure 2.24 Experiment: dc-link voltage and its reference evolution during Test A for the original (top) and the modified (bottom) algorithm.

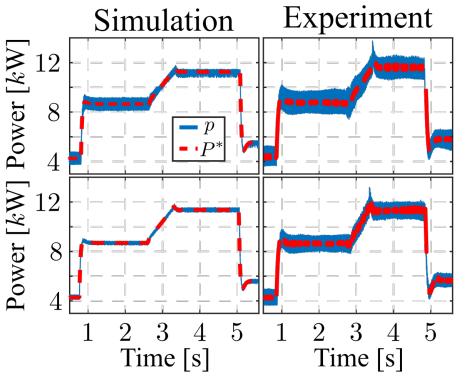

Figure 2.25 Simulation and Experiment: Evolution of the instantaneous active power and its reference for both the original algorithm (top) and the modified one (bottom).

the progressive change in v_{dc}^* is properly tracked. At the same time, Fig. 2.25 depicts the active power p and its reference p^* during the same experiment. In this case, this figure depicts the well behaviour of the inner controller, which uses the model-based direct power control, as p is regulated towards p^*. In order to validate the experimental results, some simulations are carried out under the same scenario and they are also plotted in the same figure. The simulation and experimental results are similar but for the power chattering, which is expected to be larger in the experiments due to non-modelled effects such as sensor nonlinearity, samples delay, gating dead-times, among others. The reduced chattering when using the modified algorithm can also be seen in this figure both in simulation and experiments.

Test B: Capacitor voltage balance

In order to test the behaviour of the proposed capacitor voltage balancing controller, Fig. 2.26 shows the evolution of the error signals v_{d1},v_{d2} and v_{d3} when they start at an unbalanced situation, i.e. values different from zero, in simulation and experiments for the original and the modified algorithm. Additionally, several tests have been carried out for different values of k_1, k_2 and k_3 to depict the effect the tuning of these control parameters has on the system performance. As it can be seen, the larger the control parameters, the faster the error signals are regulated towards zero, which is an expected outcome given (2.78)–(2.80), although, larger values could make the duty ratios to saturate more easily under transient conditions. Therefore, there is a tradeoff between balancing time and possible transient distortion. Nevertheless, given that a common rectifier application is not expected to alter the capacitor voltage balance externally to the balancing controller, it is recommended to select the minimum values of k_1, k_2 and k_3 that guarantee balanced operation in steady state.

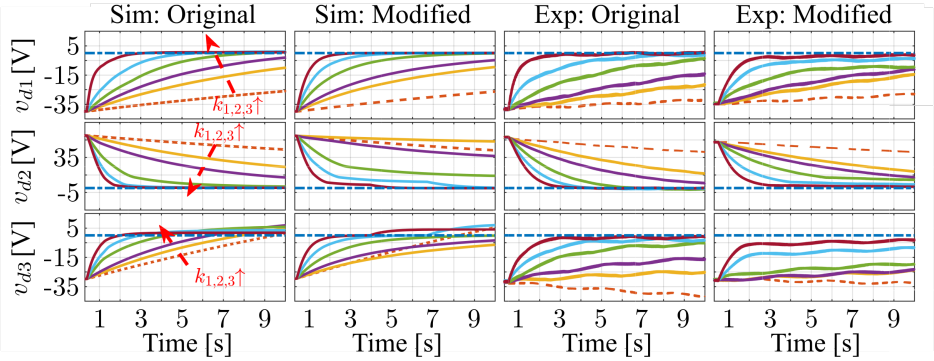

Figure 2.26 Simulation and Experiment: Evolution of the error signals v_{d1}, v_{d2} and v_{d3} when starting from an unbalanced situation for the original en the modified algorithm. Several values of k_1,k_2 and k_3 are tested simultaneously: $0, 10^{-5}, 2\cdot10^{-5}, 5\cdot10^{-5}, 10^{-4}, 2\cdot10^{-4}$. Dashed plot shows the behaviour when $k_1 = k_2 = k_3 = 0$.

Conclusions and future lines of research

This approach designs a specific controller for the balancing of the capacitor voltages in five-level DCC. The way this approach is modelled differs from the typical modulations schemes such as CB-PWM or SVM as the modulation stage is implicit in the control algorithm, given the duty ratio manipulation. Additionally, one remarkable advantage of the proposed balancing controller is that it is not affected by changes in the modulation index, and thus the range of operating points is extended in comparison with other solutions found in the literature. Furthermore, a modification in the original proposal is included in order to improve the steady-state performance without sacrificing any of the obtained benefits and with very low added complexity. Simulation and experimental results validate the achievement of common control objectives for grid-connected applications, while capacitor voltage balance is ensured. Besides, the extension of this approach to other DCC topologies is straightforward.

As future line of research, the analysis of the duty ratio saturation effect on the transient performance and possible solutions to it could derive a more robust solution. In this regard, variable values of k_1,k_2,k_3 can be a potential solution to further reduce commutations and solve the duty saturation issues, while still guaranteeing capacitor voltage balancing.

2.3.4 Integrated control and modulation for interfacing solar panels to the grid through five-level DCC

This section introduces one contribution of this dissertation that considers the previous approach to be used for a particular application placed within the context of photovoltaic energy. For this, the solar cells are disposed in such a way that four arrays are formed, whose design voltage is close to the nominal value of each capacitor of the five-level DCC. Then, they are serialized and interfaced with the grid using the stated five-level converter. The aim of this approach is to avoid the requirement of dc-dc converters to control the

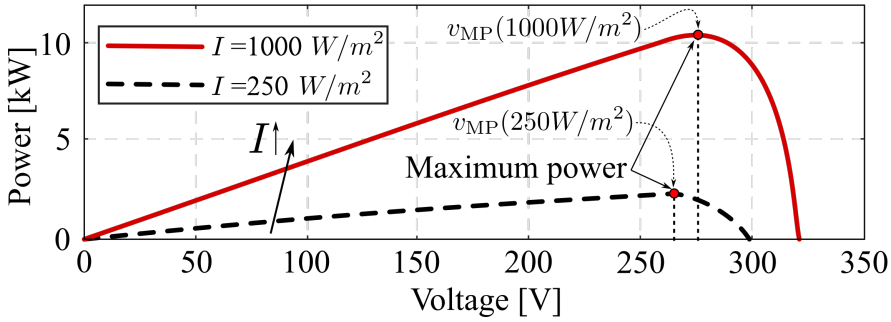

Figure 2.27 Example of power curve for two different irradiances and the corresponding maximum power point.

voltage of each solar cell group. Instead, the regulation voltage is achieved by means of the previous proposed integrated control. This particular application and extension of the five-level DCC integrated control has been presented in [118].

Maximum power point tracking principle of solar cells

The power efficiency of a solar cell highly depends on the voltage-current curve, which can vary according to the irradiance and temperature. Therefore, the maximum collectable power of the solar array is reached for a particular voltage (referred as v_{MP}). In order to improve the efficiency, it is necessary to regulate the solar cell voltage towards this value. For this, an active search of v_{MP} is carried out by the process of the so-called maximum power point tracking (MPPT), which iterates over the solar cell voltage measuring the resulting power. Generally, the power curve presents only one maximum, and thus v_{MP} can be tracked by measuring the derivative of the output power over the solar cell voltage [121]. An example of this curve is shown in Fig. 2.27 where the maximum power voltage for two different irradiances is shown. Note, however, that these ideal power curves are for a single solar cell whose voltage and power production is too low to be considered alone. For this, the solar cells are serialized until their added voltage reaches a voltage that can be handled more easily. Besides, by doing so, only one MPPT is used for the whole set of solar arrays.

Objectives

Considering the above, the following objectives are considered

- Use a five-level DCC to interface four serialized arrays of solar cells to the grid, where the value of v_{MP} for each array is expected to be close to $v_{dc}/4$.
- Avoid the requirement of dc-dc converters by directly regulating each solar cell array voltage in such a way that the MPPT is carried out.
- Manage the produced power by each solar cell array so they flow into the grid.
- Devise an approach that avoids the distortion generated by unbalanced capacitor voltages in five-level DCC.

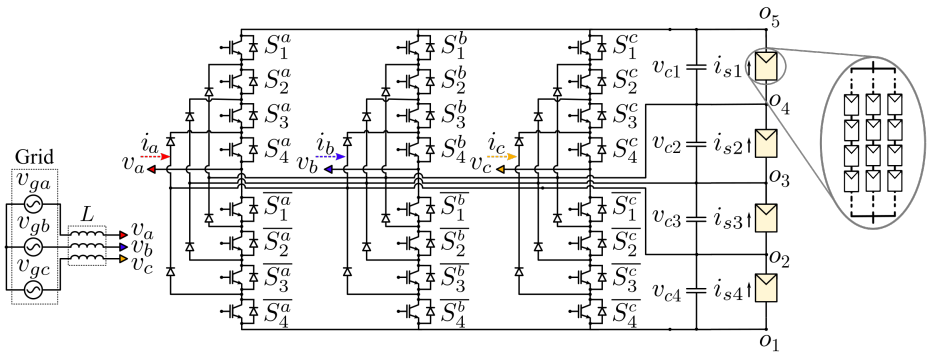

Figure 2.28 Proposed approach that interfaces four solar arrays with the grid with no need of dc-dc stage.

The proposed solution is shown in Fig. 2.28 that covers the first two stated objectives. The third and fourth objectives are covered when using the integrated control exhibited in the previous section, however some modifications have to be considered that will be exposed in the following sections.

Solar arrays

For this approach, the solar arrays are attached individually to each dc-link capacitor with no inclusion of DC-DC stage. An external MPPT (not exhibited in the current work) provides the capacitor voltage controller with the capacitor voltage reference as $v_{c1}^*, v_{c2}^*, v_{c3}^*, v_{c4}^*$. This work do not develop the MPPT implementation but assumes that the reference voltages are given externally and that they do not change abruptly (much slower dynamic than the outer loop controller). Given that the four solar arrays can output different values of active power, the current that goes through them can also be different. For this, following the same notation than (2.50)–(2.52), the following current differences are defined

$$h_1 = i_{s4} - i_{s1} \tag{2.89}$$
$$h_2 = i_{s3} - i_{s2} \tag{2.90}$$
$$h_3 = i_{s2} - i_{s1}, \tag{2.91}$$

which will be used later for the updated modelling of the capacitor voltage dynamic.

Corrected model in $\alpha\beta$ coordinates

The averaged model that uses (2.38) is still considered for this approach, although the equal capacitor voltage balance assumption can not be longer accepted given the nature of the application. For this, (2.44)–(2.45) are modified considering the definition of the error signals v_{d1}, v_{d2}, v_{d3} (2.50)–(2.52) resulting in

$$L\frac{di_\alpha}{dt} = v_{g\alpha} - \frac{v_{dc}}{4}\left(u_1 + \frac{v_{d1}}{v_{dc}}h_{d1_\alpha} + \frac{v_{d2}}{v_{dc}}h_{d2_\alpha} + \frac{v_{d3}}{v_{dc}}h_{d3_\alpha}\right) \tag{2.92}$$

$$L\frac{di_\beta}{dt} = v_{g\beta} - \frac{v_{dc}}{4}\left(u_2 + \frac{v_{d1}}{v_{dc}}h_{d1_\beta} + \frac{v_{d2}}{v_{dc}}h_{d2_\beta} + \frac{v_{d3}}{v_{dc}}h_{d3_\beta}\right), \tag{2.93}$$

where u_1, u_2 are the control signals defined in (2.57) and (2.58), and

$$h_{d1_k} = -2d_{k1} + d_{k2} - d_{k4} - 2d_{k5} \tag{2.94}$$
$$h_{d2_k} = -2d_{k1} - 3d_{k2} - d_{k4} - 2d_{k5} \tag{2.95}$$
$$h_{d3_k} = -2d_{k2} + 2d_{k4} \tag{2.96}$$

for $k = \alpha,\beta$. Note that terms $h_{d1_k}, h_{d2_k}, h_{d3_k}$ are included to correct the effect that the error signals will have on the current dynamics. Taking into account this formulation, the fourth objective is considered. It is worth mentioning that the inclusion of these terms that depend on several duty ratios will change the duty ratio obtainment shown in (2.81)–(2.82) as it will be exhibited later.

Similarly, the dynamic of the error signals v_{d1}, v_{d2} and v_{d3} is modified to include h_1, h_2 and h_3 as follows

$$C\frac{dv_{d1}}{dt} = \sum_{k=\alpha,\beta} -(d_{k5} + d_{k1})i_k + h_1 \tag{2.97}$$
$$C\frac{dv_{d2}}{dt} = \sum_{k=\alpha,\beta} -(d_{k5} + d_{k4} + d_{k2} + d_{k1})i_k + h_2 \tag{2.98}$$
$$C\frac{dv_{d3}}{dt} = \sum_{k=\alpha,\beta} d_{k4}i_k + h_3 \tag{2.99}$$

Adapted controller design

In this case, the control signals $u_3, \ldots, u_8$ follow the definition given in (2.59)–(2.64), but u_1 and u_2 have to take into account the new formulation given in (2.92) and (2.93). For this, u_1 and u_2 are reformulated as u_1' and u_2' as follows

$$u_1' = u_1 + \frac{1}{v_{dc}}(v_{d1}h_{d1_\alpha} + v_{d2}h_{d2_\alpha} + v_{d3}h_{d3_\alpha}) \tag{2.100}$$
$$u_2' = u_2 + \frac{1}{v_{dc}}(v_{d1}h_{d1_\beta} + v_{d2}h_{d2_\beta} + v_{d3}h_{d3_\beta}). \tag{2.101}$$

With this formulation, the $\alpha\beta$ current dynamic model results in

$$L\frac{di_\alpha}{dt} = v_{g\alpha} - \frac{v_{dc}}{4}u_1$$
$$L\frac{di_\beta}{dt} = v_{g\beta} - \frac{v_{dc}}{4}u_2.$$

Consequently, any well-known current controller can be implemented to define the value of u_1 and u_2 [25]. In the following, a PI current controller in rotating synchronous

reference frame dq, which has been already explained in the introduction section, is considered here as follows

$$u_d = \frac{4}{v_{dc}}\left(k_p(i_d^* - i_d) - i_q\omega_g L + k_i\int_0^t (i_d^* - i_d)d\tau\right) \tag{2.102}$$

$$u_q = \frac{4}{v_{dc}}\left(k_p(i_q^* - i_q) + i_d\omega_g L + k_i\int_0^t (i_q^* - i_q)d\tau\right), \tag{2.103}$$

where i_d, i_q are the measured phase currents in dq, i_d^*, i_q^* are their respective references, and u_d, u_q are the current control signals in dq reference frame that have to be translated to $\alpha\beta$

$$\begin{aligned} u_1 &= u_d\cos(\omega_g t) - u_q\sin(\omega_g t) \\ u_2 &= u_d\sin(\omega_g t) + u_q\cos(\omega_g t)\,. \end{aligned}$$

The outer loop control is kept the same than in the previous approach, and the current references are obtained through the instantaneous power theory as exhibited in the introduction section.

Lastly, the capacitor voltage controllers presented in (2.75)–(2.77) have to be modified taking into account the presence of h_1, h_2 and h_3, and that the controller no longer aims to regulate the error signal towards zero, i.e. equal capacitor voltages, but to a particular value defined by the capacitor voltage references. In this regard, variables v_{d1}^*, v_{d2}^* and v_{d3}^* are defined as references for the error signals

$$v_{d1}^* = v_{c4}^* - v_{c1}^*\,, \quad v_{d2}^* = v_{c3}^* - v_{c2}^*\,, \quad v_{d3}^* = v_{c2}^* - v_{c1}^*\,, \quad v_{dc}^* = v_{c1}^* + v_{c2}^* + v_{c3}^* + v_{c4}^*\,,$$

where v_{dc}^* is no longer defined by the user, but it is the result of applying the desired capacitor voltage defined by the MPPT algorithms. Consequently, the outer loop regulates v_{dc} towards v_{dc}^*, whereas the error signal controllers are formulated as follows

$$u_3 = i_\alpha \mathrm{PI}(v_{d1}^* - v_{d1}) \tag{2.104}$$

$$u_4 = i_\beta \mathrm{PI}(v_{d1}^* - v_{d1}) \tag{2.105}$$

$$u_5 = i_\alpha \mathrm{PI}(v_{d2}^* - v_{d2}) \tag{2.106}$$

$$u_6 = i_\beta \mathrm{PI}(v_{d2}^* - v_{d2}) \tag{2.107}$$

$$u_7 = i_\alpha \mathrm{PI}(v_{d3}^* - v_{d3}) \tag{2.108}$$

$$u_8 = i_\beta \mathrm{PI}(v_{d3}^* - v_{d3})\,, \tag{2.109}$$

where $\mathrm{PI}(x) = k_\mathrm{p}^\mathrm{bal}x + k_\mathrm{i}^\mathrm{bal}\int_0^t x d\tau$. The closed-loop dynamics of the error signals result in the following equations

$$\begin{aligned} \frac{dv_{d1}}{dt} &= I^2\mathrm{PI}(v_{d1}^* - v_{d1}) + h_1 \\ \frac{dv_{d2}}{dt} &= I^2\mathrm{PI}(v_{d2}^* - v_{d2}) + h_2 \end{aligned}$$

$$\frac{dv_{d3}}{dt} = I^2\text{PI}(v^*_{d3} - v_{d3}) + h_3\ ,$$

where each integral term compensates for the corresponding current unbalance h_1, h_2 or h_3, whereas the proportional terms ensure the capacitor voltage signal error tracking.

Modulation stage

Similarly to the previous approach, once $u_1,\ldots,u_8$ are determined applying the corresponding controller, the duty values $d_{\alpha j}$ and $d_{\beta j}$ for $j = 1,2,4,5$ can be obtained by reversing the control variable definitions

$$\begin{bmatrix} d_{\alpha 1} \\ d_{\alpha 2} \\ d_{\alpha 4} \\ d_{\alpha 5} \end{bmatrix} = \begin{bmatrix} -\frac{1}{4} & d^{u_3}_{\alpha 1} & d^{u_5}_{\alpha 1} & d^{u_7}_{\alpha 1} \\ 0 & -1 & 1 & 1 \\ 0 & 0 & 0 & -1 \\ \frac{1}{4} & d^{u_3}_{\alpha 5} & d^{u_5}_{\alpha 5} & d^{u_7}_{\alpha 5} \end{bmatrix} \begin{bmatrix} u_1 \\ u_3 \\ u_5 \\ u_7 \end{bmatrix} \tag{2.110}$$

$$\begin{bmatrix} d_{\beta 1} \\ d_{\beta 2} \\ d_{\beta 4} \\ d_{\beta 5} \end{bmatrix} = \begin{bmatrix} -\frac{1}{4} & d^{u_4}_{\beta 1} & d^{u_6}_{\beta 1} & d^{u_8}_{\beta 1} \\ 0 & -1 & 1 & 1 \\ 0 & 0 & 0 & -1 \\ \frac{1}{4} & d^{u_4}_{\beta 5} & d^{u_6}_{\beta 5} & d^{u_8}_{\beta 5} \end{bmatrix} \begin{bmatrix} u_2 \\ u_4 \\ u_6 \\ u_8 \end{bmatrix} \tag{2.111}$$

$$\begin{bmatrix} d^{u_3}_{\alpha 1} \\ d^{u_5}_{\alpha 1} \\ d^{u_7}_{\alpha 1} \\ d^{u_3}_{\alpha 5} \\ d^{u_5}_{\alpha 5} \\ d^{u_7}_{\alpha 5} \end{bmatrix} = \frac{1}{4v_{dc}} T_{v_d} \begin{bmatrix} v_{d1} \\ v_{d2} \\ v_{d3} \\ v_{dc} \end{bmatrix}, \begin{bmatrix} d^{u_3}_{\beta 1} \\ d^{u_5}_{\beta 1} \\ d^{u_7}_{\beta 1} \\ d^{u_3}_{\beta 5} \\ d^{u_5}_{\beta 5} \\ d^{u_7}_{\beta 5} \end{bmatrix} = \frac{1}{4v_{dc}} T_{v_d} \begin{bmatrix} v_{d1} \\ v_{d2} \\ v_{d3} \\ v_{dc} \end{bmatrix}, T_{v_d} = \begin{bmatrix} -3 & 1 & 2 & 3 \\ 1 & -3 & -2 & -1 \\ 2 & -2 & -4 & -2 \\ 3 & -1 & -2 & 1 \\ -1 & 3 & 2 & 1 \\ -2 & 2 & 4 & 2 \end{bmatrix}.$$

From (2.110)–(2.111), the $\alpha\beta$ duty ratios are obtained for levels 1,2,4 and 5. It is worth recalling from the integrated control approach that the duty ratios of level three are later determined from the duty ratio restriction $\sum_{j=1}^{5} d_{ij} = 1$ for each phase $i = a,b,c$. However, as stated in the integrated control approach, there are still four degree of freedoms associated to the values of $d_{\gamma 1}, d_{\gamma 2}, d_{\gamma 4}$ and $d_{\gamma 5}$. In the previous section, it was assumed that the error signals at steady-state are close to zero, and thus the control variables $u_3,\ldots,u_8$ are also close to zero, which means that duty ratios of levels 2 and 4 are almost not used. In this case, this is not longer valid as the control scheme implements a PI controller whose integral term may result in a bias value in steady state. Due to this, the γ duty ratio determination deserves special attention as the d_{ij} are more likely to saturate. The algorithm improvement is initially considered but with the aim of avoiding d_{ij} saturation.

In the following, a guideline to derive the values of $d_{\gamma j}$ for $j = 1,2,4,5$ is given. The boundaries of d_{ij} for each phase i are

$$\sum_{j=1,2,4,5} d_{ij} \leq 1 \tag{2.112}$$

$$d_{ij} \geq 0 \quad \text{for } j = 1,2,4,5\,. \tag{2.113}$$

On the one hand, from (2.112) one upper bound for the four levels can be formulated from each phase boundary. Defining, $d_\gamma^{\mathrm{S}} = \sum_{j=1,2,4,5} d_{\gamma j}$ and considering the reverse Clarke transformation, three limits are given

$$\text{phase a:} \quad d_\gamma^{\mathrm{S}} \leq \sqrt{3} - \sum_{j=1,2,4,5} \sqrt{2} d_{\alpha j} \tag{2.114}$$

$$\text{phase b:} \quad d_\gamma^{\mathrm{S}} \leq \sqrt{3} + \sum_{j=1,2,4,5} \left(\frac{d_{\alpha j}}{\sqrt{2}} - \sqrt{\frac{3}{2}} d_{\beta j} \right) \tag{2.115}$$

$$\text{phase c:} \quad d_\gamma^{\mathrm{S}} \leq \sqrt{3} - \sum_{j=1,2,4,5} \left(\frac{d_{\alpha j}}{\sqrt{2}} + \sqrt{\frac{3}{2}} d_{\beta j} \right). \tag{2.116}$$

On the other hand, from (2.113) one lower bound for each level j can be derived from the three phase boundaries.

$$\text{phase a:} \quad d_{\gamma j} \geq -\sqrt{2} d_{\alpha j} \tag{2.117}$$

$$\text{phase b:} \quad d_{\gamma j} \geq \frac{d_{\alpha j}}{\sqrt{2}} - \sqrt{\frac{3}{2}} d_{\beta j} \tag{2.118}$$

$$\text{phase c:} \quad d_{\gamma j} \geq \frac{d_{\alpha j}}{\sqrt{2}} + \sqrt{\frac{3}{2}} d_{\beta j}. \tag{2.119}$$

Notice that both boundaries are reflected as a set of three equations, but only the most restrictive one would apply. The solution adopted in this work goes through selecting the minimum values of $d_{\gamma 1}$ and $d_{\gamma 5}$ that fulfill (2.113), and then dividing among the three remaining levels $j = 2,3,4$ the spare value of d_γ^{S} until the upper bound is reached (2.112). The first selection pursues to reduce the commutations similarly to the previously presented algorithm improvement. The second choice is made in order to assure that levels 2,3 and 4 always appear in the output waveform, and thus avoiding large jumps, such as $d_{i2} \neq 0, d_{i3} = 0, d_{i4} \neq 0$. With this approach, saturation is pushed to the limit, and in the case some d_{ij} saturates, that would mean that either saturation was unavoidable for the given conditions or large jumps were necessary to be included. For the sake of simplicity, in the following simulations, those cases would simply be trimmed to [0,1].

In summary, the values of $d_{\gamma j}$ are determined in five steps

1. The most restrictive values of (2.112) and (2.113) are determined. For this, the minimum value of (2.114)–(2.116) is considered and referred as $d_{\gamma_{\mathrm{m}}}^{\mathrm{S}}$, while the maximum boundaries given by (2.117)–(2.119) for each level j are considered and referred as $d_{\gamma j_{\mathrm{m}}}$.

2. Levels 1 and 5 are directly assigned considering the maximum boundary: $d_{\gamma 1} = d_{\gamma 1_{\mathrm{m}}}$, $d_{\gamma 5} = d_{\gamma 5_{\mathrm{m}}}$. This is the same procedure than the improved algorithm considered in the previous approach and guarantee that, at least, two commutations are avoided.

3. The spare value of $d^{\mathrm{S}}_{\gamma_{\mathrm{m}}}$—referred as $d_{\gamma_{\mathrm{rem}}}$—is determined considering the minimum value of $d_{\gamma 2}$ and $d_{\gamma 4}$ from (2.117)–(2.119). That is,

$$d^{\mathrm{S}}_{\gamma_{\mathrm{rem}}} = d^{\mathrm{S}}_{\gamma_{\mathrm{m}}} - d_{\gamma 1} - d_{\gamma 5} - d_{\gamma 2_{\mathrm{m}}} - d_{\gamma 4_{\mathrm{m}}}.$$

4. Then, $d^{\mathrm{S}}_{\gamma_{\mathrm{rem}}}$ is divided equally among the three remaining levels (2,3,4) and added to the minimum value in order to make sure that the duty ratios of levels 2,3,4 are not zero:

$$d_{\gamma 2} = d^{\mathrm{S}}_{\gamma_{\mathrm{rem}}}/3 + d_{\gamma 2_{\mathrm{m}}} \qquad d_{\gamma 4} = d^{\mathrm{S}}_{\gamma_{\mathrm{rem}}}/3 + d_{\gamma 4_{\mathrm{m}}}$$

5. It is checked whether the previous operation was feasible, i.e. $d^{\mathrm{S}}_{\gamma_{\mathrm{rem}}} \geq 0$. If so, no change is performed; else, some restriction is violated and the corresponding duty ratio would saturate. In order to reduce this saturation impact as much as possible, it is proposed to make duty ratio of level 3 equal to zero, that is, making $d^{\mathrm{S}}_{\gamma_{\mathrm{rem}}} = 0$ in the previous equations and recalculating the values of $d_{\gamma 2}$ and $d_{\gamma 3}$.

To depict an example of this distribution, Fig. 2.29 shows a generic diagram where the cases of no saturation ($d^{\mathrm{S}}_{\gamma_{\mathrm{rem}}} \geq 0$) and saturation ($d^{\mathrm{S}}_{\gamma_{\mathrm{rem}}} < 0$) are depicted.

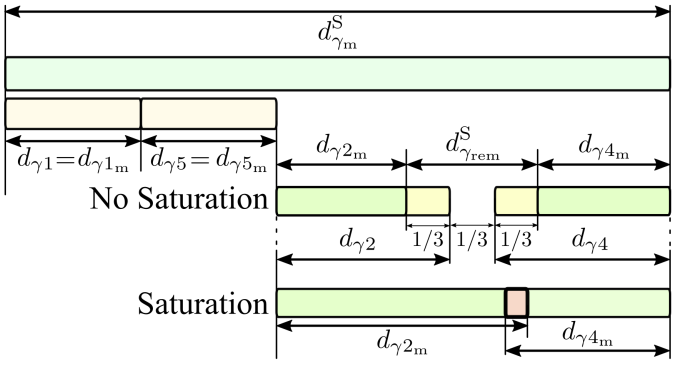

Figure 2.29 Sample of $d_{\gamma j}$ distribution for a case where no duty ratio saturation will be produced and for a case where some duty ratios will saturate.

At this point, the $d_{\gamma j}$ values for $j = 1,2,4,5$ are determined and the reverse Clarke transformation can be performed to obtain the equivalent duty ratios in abc. Lastly, the duty ratio constraint for each phase i, $\sum_{j=1}^{5} d_{ij} = 1$, is considered to obtain d_{i3}. Note that, given to the previous step 4 and when no saturation takes place, it is guaranteed that $\sum_{j=1,2,4,5} d_{ij} < 1$, and therefore the duty ratio of level 3 will not be zero.

Simulation Results

This section is devoted to present the simulation results when applying the previous algorithm to the system described in the previous section. The system and control parameters are depicted in Table 2.4. For the solar arrays, variables $v_{\mathrm{MP}_{Cp}}$ for $p = 1,2,3,4$—the

Table 2.4 5L-DCC system and controller parameters.

Parameter	Value (Units)
Inductor, L	2 (mH)
dc-link Capacitors, C	3.3 (mF)
Grid voltage	$220\sqrt{3}$ (V)
Grid frequency, f	50 (Hz)
Reactive power reference, q^*	0 (kVA)
Prop. dc-link PI controller, K_p^{dc}	0.05
Int. dc-link PI controller, K_i^{dc}	1
Prop. current controller, K_p	15
Int. current controller, K_i	25
Prop. cap. bal. controller, K_p^{bal}	0.001
Int. cap. bal. controller, K_i^{bal}	0.005

Table 2.5 Values of $v_{\text{MP}_{Cp}}$ and $p_{Cp}^{\max}$.

Cap.	Volt.	Power
C_1	260 V	5 kW
C_2	210 V	4 kW
C_3	180 V	3.6 kW
C_4	250 V	4.7 kW

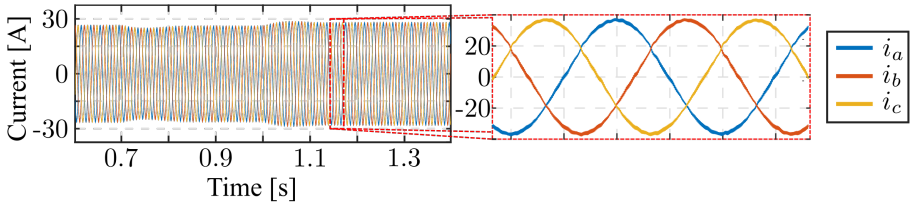

Figure 2.30 Three-phase currents in steady-state.

capacitor voltages at which the output power is maximized—are given along with the corresponding maximum power achievable $p_{Cp}^{\max}$ in Table 2.5. The solar power curves (Curve $p-V$) are emulated for each solar array p as a second-order polynomial equation with a maximum at ($v_{\text{MP}_{Cp}}$,$p_{Cp}^{\max}$) and different bias in order to simulate different behaviors.

To evaluate the evolution of the current proposal, the simulations start with $v_{cp}^* = 200$ V for $p = 1,2,3,4$ and, from $t = 0.7$ and on, these values are updated progressively until they reach $v_{\text{MP}_{Cp}}$ simultaneously at $t = 1$.

The three-phase currents at steady-state are shown in Fig. 2.30 where the zoomed area depicts the current when the system has reached steady state with its maximum power production. Besides, it can be seen that the current amplitude change along the simulation according to the obtained power. It is worth mentioning that there is a current sag at $t = 0.7$ s due to power required to increase the capacitor voltages. In this regard, it can be seen how the proposed converter starts increasing the delivered power once the capacitor voltage references have been reached at $t = 1$ s.

The output power of each solar array and the capacitor voltage evolution are shown in Fig. 2.31 and Fig. 2.32, respectively. As expected, the capacitor voltage balance controller is able to track the references while the obtained output power is maximized. Considerably

large differences in the capacitor voltage at steady-state conditions are tested, which proves the feasibility of the current proposal to track different capacitor voltages. Besides, note from Fig. 2.27 that the variation of $v_{\mathrm{MP}C_p}$ for different irradiances is far less noticeable than the change considered in this test, which proves the conservative of these simulations.

Lastly, in order to prove the effectiveness of the corrected model and consequent modifications in the duty ratios obtainment, Fig. 2.33 is plotted. Thanks to the corrected model, the capacitor voltage unbalance at steady-state has no effect on the current distortion. Indeed, the THD value is reduced, as shown in Fig. 2.33 (top), due to the increment in the amplitude of the fundamental component, as the output power is increased without generating further distortion. With regard to the output waveform, Fig. 2.33 (bottom) depicts the phase a switching state at steady-state conditions, where it can be seen that during one third of the grid period the five levels are used, whereas no large jumps are produced thanks to the proposed d_γ distribution.

Conclusions and future lines of research

This section exhibits a potential application of the developed integrated control to interface several solar arrays with the grid using only a five-level DCC. With this and considering that no dc-dc stages are required, a potential reduction in size and improved efficiency can be achieved. It is also shown that the maximum power point tracking capability is possible to achieve by providing this algorithm with the references for the capacitor voltage values.

The potential lines of research includes the extension of this approach to different topologies and number of levels, the analytical study of the duty ratio saturation and how the d_γ distribution affect them, experimental verification, and the effect the ground coupling or current leakage of solar arrays may have on the performance of this approach, among others. Additionally, the inclusion of high-efficient isolating DC-DC stages could be also considered. With this, the solar arrays can be interfaced with the dc-link capacitors in such a way that, combined with the voltage regulation capabilities of this approach, the application offers a wide flexibility in the voltage range of the operating point.

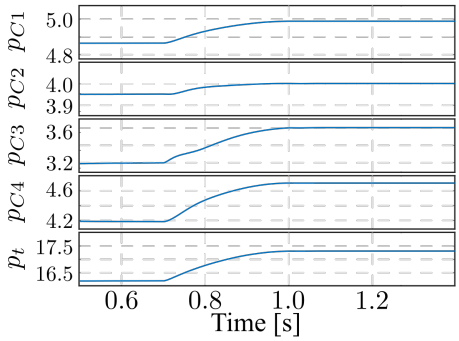

Figure 2.31 Evolution of the power extracted from each solar array ($p_{Cp} = v_{cp} i_{sp}$) in kW.

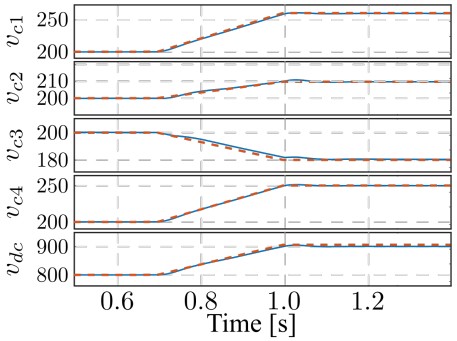

Figure 2.32 Evolution of the capacitor voltages (solid) and their references (dashed) in V.

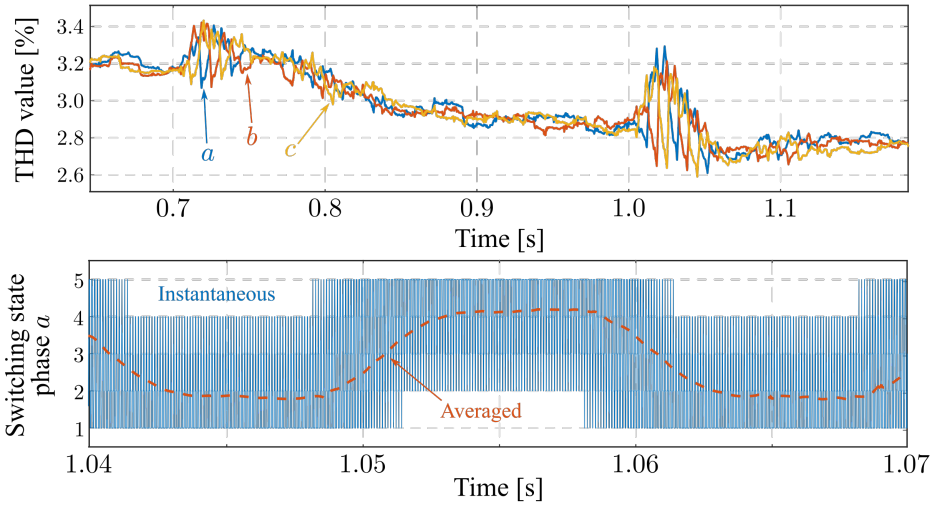

Figure 2.33 THD value of the three-phase currents during the test considered (in % of current amplitude) (top); and switching state of phase a (Output waveform) and its averaged value (bottom).

2.3.5 Thermal analysis of the integrated modulation and control approach. Comparison with the improved algorithm

This section presents a contribution of this work that focuses on analyzing the effect the integrated control and modulation approach presented in Sect. 2.3.3 has on the conductive losses [119]. Besides, the algorithm improvement, also presented in Sect. 2.3.3, is included in the analysis and used for comparison. With this, some conclusions are drawn on which approach is more feasible to increase the life expectancy of the switching devices. The switching losses are not included in this analysis due to its dependence with the operating conditions, as it is explained later.

Thermal management

Device temperature concern is leading a new concept of power converter design known as thermal management [122]. This is due to the undesired effects that high temperature or temperature changes may have on power device reliability and durability. Consequently, temperature is a key point that has to be taken into account in order to extend the expectancy of power device lifetime [123]. The current going through each power device creates a power flow that yields cyclic heating and cooling intervals. Considering the different thermal expansions coefficients of the components inside the power device, these intervals create mechanical stress that are translated to aging and, consequently, reduced lifetime expectancy [124]. Therefore, it is critical to reduce its magnitude in order to reduce long-term expenses [125]. In this sense, active thermal control (ATC) is a technique that takes into account these effects and modifies the overall performance in such a way that the amplitude of these cycles or the averaged temperature level are decreased.

In the case of multilevel power converters, this is of special importance as, depending on the topology, some semiconductors might be closed longer than others which entails more conduction losses and therefore bigger thermal aging effects. As a consequence, these devices are more likely to reach its lifetime end than the others, increasing the cost of maintenance. As a result, several studies have been carried out to consider the thermal management into the control of multilevel converters [126–128].

The approach presented in Sect. 2.3.3 uses all levels within a switching period, whereas its improvement can skip some of them. Using several levels could yield higher switching losses than other known approaches for multilevel converters, although it could make the dissipated power to be more equally distributed among the semiconductors, reducing the thermal cycles and aging. The switching losses highly depend on the switching frequency, the point of operation and how the levels are sequenced in the output within a switching period. However, in multilevel converters, as the device blocking voltage is reduced by the introduction of several levels, their magnitude for every device is considerably reduced in comparison with two level topologies that hold the same dc-link voltage. Nevertheless, a tradeoff comparison dependant on the operating point has to be made to determine which is the most suitable approach. Because of this, the switching losses have not been considered in this analysis as it would not yield any straight conclusion. Moreover, using a turn-off snubber circuit translates part of the power dissipation due to switching to the external circuit, and thus it reduces the heating caused by the switching of the device.

This section exhibits the two proposed approaches and compares them in terms of thermal effects.

Conduction losses

The considered modulation approaches will yield different losses profiles as the conducting time and turning-on/off cycles of the power devices differ depending on the levels used. The higher the duty ratio, the higher the conducting time of the power devices. Therefore, the analysis will focus on a generic phase i and the conduction losses of the four upper semiconductors $\{S_1^i, S_2^i, S_3^i, S_4^i\}$ considering that the lower ones will have a symmetrical behaviour. Also, no dead time is considered as it can be emulated as an extension of the duty ratios [129].

It is also worth to mention that the current will not always go through the switching device but through the anti-parallel diode sometimes—whenever the phase current $i_i > 0$—which would change the losses profile. However, considering the periodical behaviour of the phase current and that this section aims for a comparative analysis, only the losses generated in the switching devices are considered, i.e. only when $i_i \leq 0$. In this way, a variable called switching device usage ${S_n^i}^u$ can be defined as follows

$$
\begin{aligned}
S_1^{i\,u} &\doteq \begin{cases} d_{i5}|i_i| & \text{if } i_i \leq 0 \\ 0 & \text{if } i_i > 0 \end{cases} \\
S_2^{i\,u} &\doteq \begin{cases} (d_{i5}+d_{i4})|i_i| & \text{if } i_i \leq 0 \\ 0 & \text{if } i_i > 0 \end{cases} \\
S_3^{i\,u} &\doteq \begin{cases} (d_{i5}+d_{i4}+d_{i3})|i_i| & \text{if } i_i \leq 0 \\ 0 & \text{if } i_i > 0 \end{cases} \\
S_4^{i\,u} &\doteq \begin{cases} (d_{i5}+d_{i4}+d_{i3}+d_{i2})|i_i| & \text{if } i_i \leq 0 \\ 0 & \text{if } i_i > 0\,, \end{cases}
\end{aligned}
\tag{2.120}
$$

which represents the averaged current that goes through the device S_n^i for $n = 1,2,3,4$ and $i = a,b,c$ over a switching period. The greater this value, the greater the conduction losses. To derive an estimation of the module's lifetime, the Coffin–Manson–Arrhenius model [130] can be used, which provides the expected number of cycles to fail (N) as a function of the heating cycle and amplitude of it. This model highlights that the greater the temperature range of the cycle or the maximum reached temperature, the smaller the value of N. Consequently, reducing these two parameters is a way to provide thermal management of the devices, extending its expected lifetime span.

In order to perform the comparison, the duty ratio values of each modulation approach have to be obtained. For this, it is worth recalling that the main differences between the two considered modulations are in the values of $d_{\gamma j}$, which, when transformed to the abc frame, modify all duty ratios of the corresponding level $j = 1,2,4,5$. Considering steady-state conditions with balanced capacitor voltages,

$$
\begin{aligned}
u_\alpha &= u_1 = \sqrt{\frac{3}{2}} U \cos(\omega t),\ i_\alpha = \sqrt{\frac{3}{2}} I \cos(\omega t + \sigma) \\
u_\beta &= u_2 = \sqrt{\frac{3}{2}} U \sin(\omega t),\ i_\beta = \sqrt{\frac{3}{2}} I \sin(\omega t + \sigma) \\
u_{3,\ldots,8} &\approx 0\,,
\end{aligned}
\tag{2.121}
$$

where $U \in [0,2]$, I are the amplitude of the control signal and the phase currents in abc, respectively; σ is the phase-shift of the currents; and ωt is the grid angle. Note that U is proportional to the modulation index m as $U = 2m$, where $U = 2$ is the maximum instantaneous output voltage achievable (i.e. $m = 1$). Given that, from (2.121), variables $d_{\alpha j}$ and $d_{\beta j}$ for $j = 2,3,4$ are equal to zero the following switching device usages (2.120) are obtained

$$
S_n^{i\,u} = \left(T_{\alpha\beta\to i}[d_{\alpha 5}\, d_{\beta 5}]^{\mathrm{T}} + \sum_{j=\{6-n,\ldots,5\}} d_{\gamma j}/\sqrt{3} \right) |i_i| \quad \text{for } n = 1,2,3,4 \tag{2.122}
$$

$$d_{\alpha 5} = \frac{u_1}{4} \tag{2.123}$$

$$d_{\alpha 1} = -\frac{u_1}{4} \tag{2.124}$$

$$d_{\beta 5} = \frac{u_2}{4} \tag{2.125}$$

$$d_{\beta 1} = -\frac{u_2}{4}, \tag{2.126}$$

where $T_{\alpha\beta\rightarrow i}$ is the transformation vector of duty ratios from $\alpha\beta$ to phase i, and Eqs. (2.123)–(2.126) were defined from the control output, as it has been shown in Sect. 2.3.3. Eq. (2.122) exhibits that the differences in the device usage within the same phase at steady state relies mainly on the value of $d_{\gamma j}$. The lower its value for level j, the more similar the usage between the devices $n < 6-j$ and the devices $n \geq 6-j$. It is worth mentioning that the device usage exhibited in Eq. (2.122) is referred only to the four upper semiconductor devices, which explains their only dependence on d_{k5}, as it is the duty ratio that turns them all on. Were the four lower semiconductor devices to be considered instead, the device usage would be dependant on d_{k1}.

Following the presented approaches, the value of $\sum d_{\gamma j}|i_i|$ for each possible value of n is:

· Approach 1 (App1):

$$\sum_{j=\{6-n,\ldots,5\}} d_{\gamma j}|i_i| = \sum_{j=\{6-n,\ldots,5\}} k_{\gamma j}|i_i| \tag{2.127}$$

· Approach 2 (App2):

$$\sum_{j=\{6-n,\ldots,5\}} d_{\gamma j}|i_i| = \begin{cases} d_{\gamma 5}^{\text{App2}}|i_i| & n \leq 2 \\ (d_{\gamma 5}^{\text{App2}} + d_{\gamma 3}^{\text{App2}})|i_i| & n > 2 \end{cases}, \tag{2.128}$$

where Approach 1 is the one that considers fixed values of $d_{\gamma j}$ (values $k_{\gamma j}$) for $j = 1,2,4,5$, while Approach 2 defines the value at every instant, and thus it will be referred as $d_{\gamma j}^{\text{App2}}$ for $j = 5,3$—note that $d_{\gamma j}^{\text{App2}}$ for $j = 2,4$ are equal to zero due to the steady-state condition of $d_{kj} = 0$. The values of the first approach are selected by the user, but the second ones are given from the approach algorithm. Notice that $d_{\gamma 3}$ is obtained from applying the Clarke transformation to the restriction of $\sum_{j=1}^{5} d_{ij} = 1$ which results in the condition $\sum_{j=1}^{5} d_{\gamma j} = \sqrt{3}$, as exhibited in Sect. 2.3.4. Consequently, the device usage can be obtained from using these values into Eq. (2.122) and considering steady-state conditions (2.121). The usage is proportional to the current amplitude, so it can be normalized for comparative purposes ($I = 1$).

In the following, the device usage of the switching device S_4^i is considered as it is the most used device among the four upper devices (similarly, S_5^i would be the corresponding one among the four lower devices). Assuming steady-state conditions and the parameters shown in Table 2.6, the device usage ${S_4^i}^u$ is depicted in Fig. 2.34 for different values of σ and for the two considered approaches. From this image, it can be seen that the ${S_4^i}^u$ values for approach 2 are generally greater than those for approach 1, which means that approach

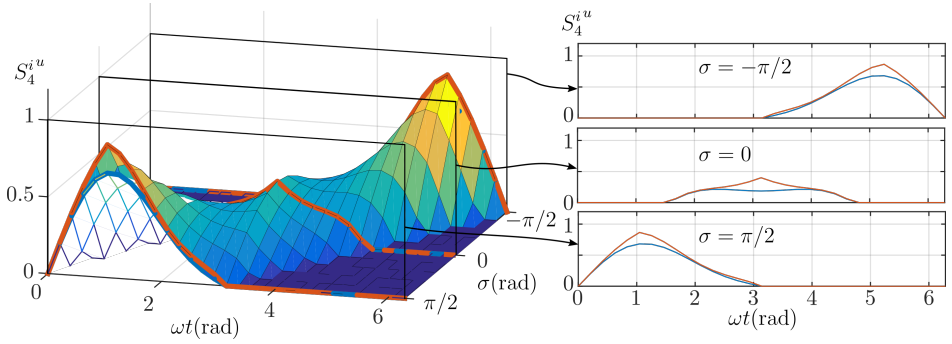

Figure 2.34 Usage S_4^{iu} for $U = 1.60$ and normalized current along a grid period and different values of σ. Approach 1 is depicted as a mesh (blue) while approach 2 is depicted as a surface (red).

1 achieves lower usage when compared to the second approach. Indeed, the use of more levels in the output waveform reduces the time each of those levels are used, which, in steady state, results in having a more spread usage among the switching devices, and thus, lower conductive losses.

Table 2.6 Equation parameters used for the S_4^{iu} computation shown in Fig. 2.34.

Par.	Value	Par.	Value
$k_{\gamma 1}$	$(\sqrt{3}-0.3)/2$	Contr. signal Ampl., U	1.6
$k_{\gamma 2}$	0.1	Current Ampl., I	1 A
$k_{\gamma 4}$	0.1	Current phase-shift, σ	$[-\pi/2,\pi/2]$ rads
$k_{\gamma 5}$	$(\sqrt{3}-0.3)/2$		

On the other hand, Fig. 2.35 depicts the results of integrating S_4^{iu} over a grid period as a function of σ for different values of U for the first approach (App1), the second one (App2) and, for comparative purposes, for the two-nearest-level modulation (2L). The latest is the result of using only the two nearest levels around u_i, i.e. the only $d_{ij} \neq 0$ are for $j = \text{floor}(u_i + 3)$ and $j = \text{ceil}(u_i + 3)$. Notice that σ is related to the power factor (PF) as PF$\approx cos(\sigma)$ in ideal steady-state conditions. It can be clearly seen that the first approach yields lower values of the integral of the usage, which reinforces the statement that the first approach achieves lower conductive losses, and thus, better thermal management. In order to depict the different performance of the approaches and the two-nearest-level modulation, Fig. 2.36 depicts the duty ratios of each switching device $S_{1,\ldots,4}^{i}$ with $U = 1.6$.

In general terms, over a grid period, the PF barely modifies the value of S_4^{iu}, and it is clear that the 2L approach yields the worst result in terms of usage. This is due to the fact that the 2L approach uses only two levels, which results in larger values of the duty ratio of the levels involved, which indeed creates large differences in the semiconductor usages. Besides, 2L approach does not tackle the capacitor voltage balance issue, but it was considered in this analysis for comparative purposes. The differences between App1

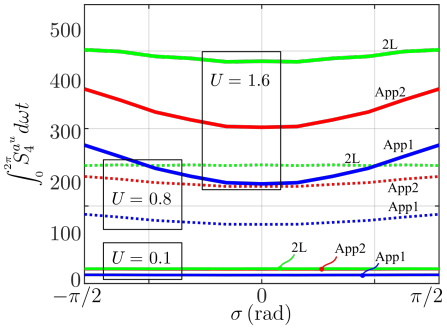

Figure 2.35 Integral of the S_4^{iu} over a grid period as a function of σ and three different values of U for the three approaches.

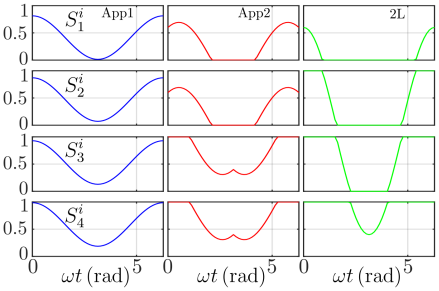

Figure 2.36 Duty ratios of switching devices $\{S_1^i, S_2^i, S_3^i, S_4^i\}$ for the three considered approaches with $U = 1.6$.

and App2 can be seen in the usage of S_3^i and S_4^i compared to S_1^i and S_2^i. The computation of $d_{\gamma j}$ to suppress some commutations results in bigger values of d_{i3}, which increases the usage of S_3^i and S_4^i, resulting in a more uneven usage distribution when compared to App1.

Simulation results

Lastly, some simulations are carried out to further depict these differences. The used controllers and control parameters are the same than those shown in Sect. 2.3.3. The circuit parameters are presented in Table 2.7, and three different tests are carried out to evaluate the steady-state performance:

1. $q^* = -25$ kVA, $R = \infty\,\Omega$ (which yields $p^* = 0$ W)
2. $q^* = -10$ kVA, $R = 43\,\Omega$ (which yields $p^* = 15$ kW)
3. $q^* = -5$ kVA, $R = \infty\,\Omega$ (which yields $p^* = 0$ W)

Table 2.7 Simulation and circuit parameters.

par.	Value	par.	Value
Filter Inductance, L	2 mH	dc-link capacitors, C	3.3 mF
dc-link volt. ref., v_{dc}	800 V	Grid Volt.	220 V_{rms}
Cap. volt. bal. par., k_1,k_2,k_3	$2{\cdot}10^{-4}$	Switching freq., f_s	10 kHz

The simulations are summarized in Fig. 2.37 where the main differences in the two approaches and the 2L approach can be seen. The switching states are depicted in the upper graph where it can be seen that, whereas the Approach 1 (App1) uses all levels every switching period, Approach 2 (App2) skips some of them. Similarly, the upper-mid graph shows the current through S_4^a including the anti-parallel diode. Notice again that Approach 1 conducts every period, in contrast to Approach 2. However, by looking at the lower-mid graph, where the conduction losses are depicted, using the integrated IGBT

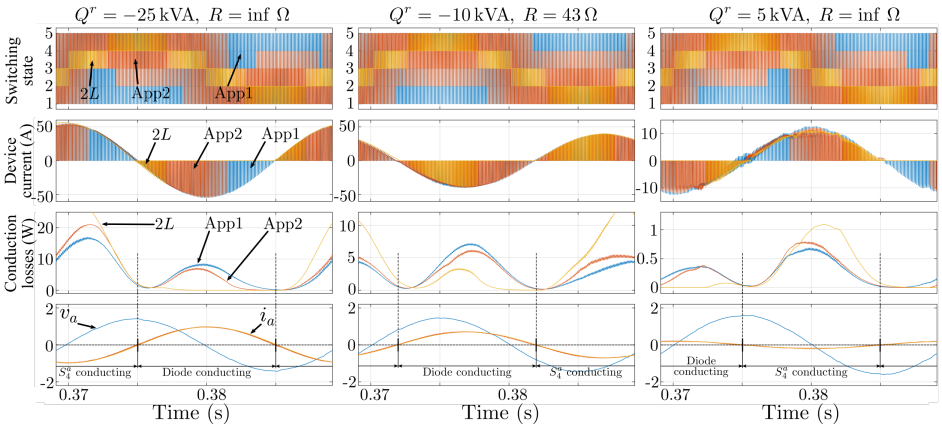

Figure 2.37 Simulation results for the three test considered in phase a. Upper graphs show the switching states; upper-mid graphs show the current through the device S_4^a; lower-mid graphs show the conduction losses computed in simulation; and lower graphs show the normalized current and output voltage for phase a.

model 5SNA1600N170100 for parasitic parameters determination, it can be seen that the overall conduction losses are worse for Approach 2 when the current goes through the device ($i_a \leq 0$). Considering this, it can be said that Approach 1 offers a better profile for the conduction losses that, in global terms, will yield less thermal stress for the device. On the other hand, the conduction losses when the current goes through the diode is worse for the Approach 1 than the Approach 2, although diodes has usually longer life expectancy and less voltage drop than the switching devices. Therefore, its impact on the equipment life expectancy is less strident. In any case, both approaches offer a better profile for the conduction losses than the two level modulation approach according to Fig. 2.35 and Fig. 2.37. Not only its integral is smaller but also the conduction losses are more spread among the switching devices, reducing the thermal cycling effect and approximating the lifetime end of all switching devices.

Conclusions and future lines of research

This brief analysis exhibits one additional benefit of the proposed integrated control and modulation approaches when compared with the well-known two-nearest level (2L) modulation, which is that the conduction losses are more equalized among switching devices. It is also worth mentioning that the 2L modulation approach was included here for comparative purposes, although this modulation could not be used alone in a five-level DCC as the capacitor voltage balancing issue is not taken into account. It is also worth mentioning that, as a result from this analysis, the modified algorithm of the integrated control and modulation approach yields worse conduction losses profile when compared with the original algorithm. However, the modified algorithm would yield lower switching losses which might compensate the bigger conduction losses depending on the operating conditions. In any case, the more suitable approach would be determined by the operating

conditions and the target application, and thus they have to be evaluated considering both losses profiles.

Further comparisons with other well-known approaches with balancing capabilities, such as some variations of SVM, could be considered as future lines of research, including those optimal modulations that take the conduction losses into account (such as some particular formulations of FCS-MPC). Furthermore, another line of research could consider this analysis as a base to develop an active thermal management of the switching devices of a five-level DCC using the degree of freedom related to $d_{\gamma j}$ exhibited in the integrated control and modulation.

2.3.6 Optimal modulation based on mixed-integer linear programming

Despite the fact that the previous solutions and analysis came up with a feasible solution for five-level DCC, they have not been designed to achieve optimal results. In fact, the switching losses are not negligible compared to other approaches, and they can even outweigh the benefits exposed in the previous section.

For certain applications, it may be necessary to aim for better solutions that achieve lower switching losses or reduced current distortion. In this line, there are some techniques that optimize a certain performance index, as in [131] where genetic algorithms are used to eliminate specific harmonics from the output voltage; the approach presented in Sect. 2.2.5 [93] where hybrid dynamical systems theory is used to obtain a new control law for three-level converters with stability guarantee; or the well-known finite control-set model predictive control (FCS-MPC) where knowledge about the system is used to select the more appropriate discrete state according to a model-based prediction [89]. In order to guarantee that the optimal position is selected among the finite set of possible switching states, most of these approaches use a weighted cost function that takes into account some performance indicators and the system model. Thanks to this, some performance indicators can be prioritized over others by changing the weights. However, in contrast to other common approaches, such as SVM or CB-PWM, they allow commutations only at the sampling time instants, where the cost function is evaluated, and thus, they lack the ability of allowing commutations at any time instant inside the sampling period. Consequently, they usually need larger sampling frequencies to obtain similar switching performance, in addition to higher computational effort than those that are PWM-based.

This section presents a contribution of this dissertation regarding an optimal formulation for multilevel converter modulation based on mixed-integer linear programming extracted from [132], which has been presented in [117]. A distinctive feature of it is that it considers averaged models for the modulation, i.e. the duty ratios, which allows the modulation to perform similarly to PWM-based approaches in terms of switching ripple. With this, an optimal solution can be derived without abandoning the main benefits of PWM solutions. In contrast to the above-mentioned optimal solutions, where the switching states are computed directly, the resolution of the optimization problem determines which levels per phase are used in the current switching period, i.e. which duty ratio $d_{ij} \neq 0$ for each phase $i = a,b,c$. This method does not need to approximate the model in discrete time, which is a notable difference from the typical MPC [133].

Optimization problem formulation

The optimization formulation is developed for the modulation stage, which is in charge of commanding the switching devices in such a way that the current/power controller output is properly carried out in the system. For this, the formulation is based on the averaged model of the system that uses the duty ratio d_{ij} concept, which has been presented in Sect. 2.1.1. Due to the nature of multilevel converters, the capacitor voltage balancing issue has to be addressed as well. Then, the optimization considers as constrains the fulfillment of the desired output voltage (controller output) and the capacitor voltage balance, while the output of such formulation are the duty ratios of every phase i and level j. The optimality is sought in reducing the number of commutations as much as possible, in order to reduce the switching losses, at the same time that some undesired solutions are weighted to be avoided as far as possible. In the following, the optimization problem that has to be solved every sampling time is formulated along with its inputs, contraints and outputs.

Constraints

Considering that the formulation uses the duty ratios concept, the constraints are the following ones

- The sum of the duty cycles for each phase has to be one (equality constraints)

$$\sum_{j=1}^{5} d_{ij} = 1;\ i = a,b,c. \tag{2.129}$$

- The outputs of the power controller ($u_1 = u_\alpha, u_2 = u_\beta$) transformed to abc (referred as η_a, η_b, η_c) have to be attained (equality constraints). Accordingly,

$$\begin{bmatrix} \eta_a \\ \eta_b \\ \eta_c \end{bmatrix} = T_{\alpha\beta\rightarrow abc} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{2.130}$$

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} \eta_a \\ \eta_b \\ \eta_c \end{bmatrix} + x = \begin{bmatrix} -2d_{a1} - d_{a2} + d_{a4} + 2d_{a5} \\ -2d_{b1} - d_{b2} + d_{b4} + 2d_{b5} \\ -2d_{c1} - d_{c2} + d_{c4} + 2d_{c5} \end{bmatrix} \tag{2.131}$$

  where x is the degree of freedom that results from the homopolar components, i.e. the $d_{\gamma j}$ values in the integrated control and modulation approach. For the current approach, the $d_{\gamma j}$ values are no longer considered, and variable x is used instead, which will be considered in the optimization formulation. Note that with this formulation, the homopolar component is no longer separated into four variables as it was the case of the integrated control and modulation approach, but represented with only one variable, that is x. In this way, the non-zero duty ratio values that input the modulator can be managed more easily.

- The balancing error signals v_{d1}, v_{d2}, v_{d3} are imposed to go to zero monotonically, i.e. making $|dv_{d_p}/dt| \leq 0$ (inequality constraint) for each error signal $p = 1,2,3$. Since the optimization formulation requires a generic formulation and the sign of

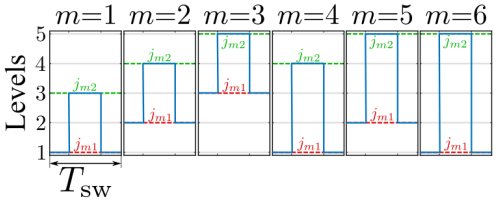

Figure 2.38 Large jumps index sample.

Table 2.8 Large jump notation.

Index m	Levels (j_{m1},j_{m2})	Index q_m
1	1, 3	1
2	2, 4	1
3	3, 5	1
4	1, 4	2
5	2, 5	2
6	1, 5	3

each v_{d_p} is unknown initially, the eight possible cases, corresponding to the eight combinations of signs, have to be considered.

Cost function

The cost function should be formulated in such a way that it reflects the objectives pursued for the converter from a practical point of view. For this, the optimal result should attend the following considerations

- Minimization of the number of commutations, i.e. the duty ratios d_{ij} that are different from zero. With this, the switching losses are reduced as much as possible.
- Some sets of duty ratios are not desired and they should be penalized. These are the cases of what is referred as large jumps from now on, that is $\exists k_1, k_2 \neq 0 \in \mathbb{N}$ s.t. $d_{i(j-k_1)} \neq 0$, $d_{ij} = 0$, $d_{i(j+k_2)} \neq 0$. Considering that the levels whose duty ratios are not zero will be sequenced by the modulator, it is not desired to have transitions between two non-consecutive levels as they introduce larger output voltage changes, more voltage stress on the switching devices, and larger current ripples. This consideration could be introduced as a constraint, but it may lead to an infeasible optimization problem. Hence, they are included here in the cost function as a penalization.

The first consideration is taken into account by introducing a set of integer variables $s_{ij} \geq 0$ for every phase i and level j in such a way that s_{ij} must be equal to one if $d_{ij} \neq 0$. By imposing s_{ij} to be integer and

$$s_{ij} - d_{ij} \geq 0; \quad s_{ij} \geq 0, \tag{2.132}$$

the value of s_{ij} is forced to be greater than one if $d_{ij} > 0$. Thanks to this, the commutation minimization can be sought by defining the following term of the cost function

$$f_{\text{cost}_1} = \sum_{i=a,b,c} \sum_{j=1}^{5} s_{ij}. \tag{2.133}$$

The second consideration can be included in the cost function as follows. Firstly, the large jumps are classified using the index m: there are six possibilities (depicted in Fig. 2.38, where the jumps are depicted from lower levels to higher ones, but the reverse case

follows the same notation) whose notation and levels involved are shown in Table 2.8. Secondly, they have to be detected, and thirdly, penalized in the cost function. Using variables j_{m1} and j_{m2} for the outer levels in the considered jump, the detection stage for phase i must search for the occurrence of $d_{ij} \neq 0$ for $j = j_{m1}$,j_{m2} and $d_{ij} = 0$ for $j_{m1} < j < j_{m2}$, which would mean that no level is active between the outer levels j_{m1} and j_{m2}. This can be accomplished by introducing two additional integer—in fact, binary—variables r_{im}, p_{im} for $i = a,b,c$ and $m = 1,\ldots,6$ and two additional constraints. Variables r_{im} are used to detect when the border levels (j_{m1},j_{m2}) are both active for the solution candidate under consideration, while variables p_{im} are used to detect if, additionally to $r_{im} = 1$, the intermediate levels are all inactive. In general terms, these two constraints are expressed for every $m = 1,\ldots,6$ and $i = a,b,c$ as:

$$s_{ij_{m1}} + s_{ij_{m2}} - r_{im} \leq 1;\ r_{im} \geq 0 \tag{2.134}$$

$$r_{im} - p_{im} - \sum_{j=j_{m1}+1}^{j_{m2}-1} s_{ij} \leq 0;\ p_{im} \geq 0 \tag{2.135}$$

In this way, the penalization for large jumps can be included in the cost function by penalising the existence of $p_{im} = 1$. Furthermore, an additional integer variable q_m is used to penalise larger jumps by making it equal to the number of additional switches this large jump implies, that is, $q_m = j_{m2} - j_{m1} - 1$ (also shown in Table 2.8). In this way,

$$f_{\text{cost}} = f_{\text{cost}_1} + \sum_{i=a,b,c} \sum_{m=1}^{6} p_{im} q_m. \tag{2.136}$$

In summary, the optimization problem formulation and the involved variables are depicted in Fig. 2.39. Additionally, an example of the variables values associated with a particular case is given for the sake of clarity.

Optimization problem

On the one hand, with this cost function formulation, the resulting problem has 67 unknowns:

- 15 variables d_{ij}.
- 15 variables s_{ij}.
- 6 variables r_{im} for each phase $i = a,b,c$: 18 variables.
- 6 variables p_{im} for each phase $i = a,b,c$: 18 variables.
- The variable x associated with the modulation.

On the other hand, there are six equality constraints (Eqs. (2.129) and (2.131)) and fifty-four inequality constraints (Eqs. (2.132), (2.134) and (2.135), and the derivative of the capacitor voltage errors). Besides, the cost function and the constraints are linear, and thus a linear mixed-integer optimization problem is formulated.

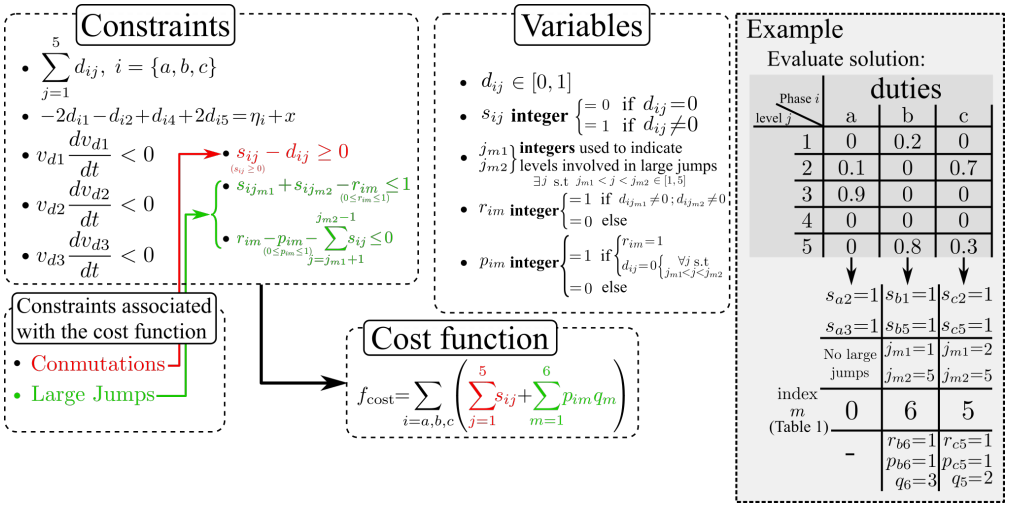

Figure 2.39 Optimization problem and example of codification for one point.

As it was stated at the beginning of this section, this optimization is carried out in the modulation stage, which means that the current/power controllers have already computed the control signals (referred as u_1, u_2 or u_α, u_β in previous sections) in such a way that the dc-link voltage value and power references are tracked. However, the previous optimization problem has a large computational burden to be implemented online in an acceptable sampling rate, and therefore it is proposed the use of look-up tables (LUTs). For this, a steady-state simulation over a grid period considering normalized state variables with N sampling instants is carried out and the resulting control signals are stored. Then, the optimization problem is solved offline with the MATLAB® Optimization Toolbox, function `intlinprog`, using these control variables as inputs for every sampling instant. The resulting duty ratios are then stored in the LUTs for further online implementation. Due to the fact that the constraints related to the voltage errors v_{dp} depend on the sign of them, and these signs can change during online operation, even at steady-state conditions—the error signal would fluctuate around 0—, eight optimization problems are solved, one for each combination of these signs, and eight LUTs are stored.

At this point, the optimization problem has been solved offline under steady-state conditions for N different points considering eight possible combinations of the voltage error signals. The next section proposes a procedure for the use of the resultant tables in the online control law.

Control law implementation

According to the information obtained from the steady-state simulations and the offline resolution of the optimization problem, each table is filled with the solution of the optimization problem—the values of d_{ij} and the x value—for N sampling instants over a grid period. Given the fact that u_α and u_β are assumed to be sinusoidal under steady-state conditions, the LUT can be indexed by the angle $\theta = \arctan(u_\beta/u_\alpha)$. In the following, some aspects for the use of these LUTs during online operation are explained: 1) row

selection, 2) Lookup table interpolation and 3) steady-state improvement in order to further reduce the number of commutations.

Row selection

Once the combination of sign(v_{d1}), sign(v_{d2}) and sign(v_{d3}) is known, the corresponding LUT can be selected. Then, it is necessary to locate the row corresponding to the stored information which is closer to the current state of the system. For this, the argument of u_α,u_β is used as the index variable, and hence the row with the closest angle value to this one will be chosen. Consequently, the row selection will only depend on the output of the current (or power) controller u_α,u_β. The fundamentals behind this is that under steady-state conditions for nominal values of the system, the state variables are expected to behave similarly to the simulation, and thus this approximation can be made.

Lookup table interpolation

Considering the discrete nature of the gathered samples in the LUT, the selected row will not correspond exactly to the measured data, and therefore, an interpolation algorithm must be used to derive the duty ratio values. A usual linear interpolation procedure could be applied but in this way some hard constraints could be violated. For this, a particular interpolation procedure is applied, whose objectives are ordered in descending priority as follows

1. The sums $\sum_{j=1}^{5} d_{ij}$ must be equal to 1 for $i = a,b,c$. This is a requirement for the modulation and cannot be violated.
2. Variables d_{ij} must lay between 0 and 1. This restriction is derived from the definition of duty ratio, whose value has to be within this range in order to be feasible. Failing to comply with it would introduce distortion in the controlled variables.
3. Values u_α, u_β must be accomplished according to (2.130)–(2.131).
4. The voltage balance must be fulfilled. This objective is important but can be left unattended during some transients in the case its fulfillment opposes the fulfillment of any of the above objectives.

Considering the above, the following procedure is used. It is obtained from the LUT which duty ratios d_{ij} are different from zero, i.e. the levels j of those nonzero duties for each phase i. It has been observed that, as a result of the optimization, in most sampling instants there is a phase—referred as i_0—that is fixed at one level without switching, while the other two—referred as i_1 and i_2—usually commute using only two levels not necessarily consecutive. There are some marginal cases where there is no phase fixed at one level, and they are obviated in this interpolation procedure without affecting the general system performance as it will be shown later. Due to this assumption, the value of x can be determined using (2.131) by imposing that this characteristic is present in the result, i.e. detect the phase i_0 and level j whose $d_{i_0 j} = 1$ in the LUT, and then obtain the value of x in (2.131) that achieves it. Once x is known, the values of u_{i_1} and u_{i_2} can also be computed using (2.131). Lastly, u_{i_1} and u_{i_2} are fulfilled considering only the nonzero duty ratios obtained from the LUT for each phase i_1 and i_2. Considering that it has been assumed that there is only two nonzero duties in the LUT for phase i_1 and i_2, the resultant

duty cycles are unequivocal considering the objectives 1,2 and 3 listed. Finally, it may occur that the previous procedure yields some duty cycles outside the interval $[0,1]$, which is infeasible because of the second objective considered. In such cases, the voltage-balance objective is obviated, as stated is the last objective, and the corresponding u_i is achieved by distributing it between the two nearest levels—the levels that are the closest integers to u_i. A simplified control scheme of the proposal is depicted in Fig. 2.40.

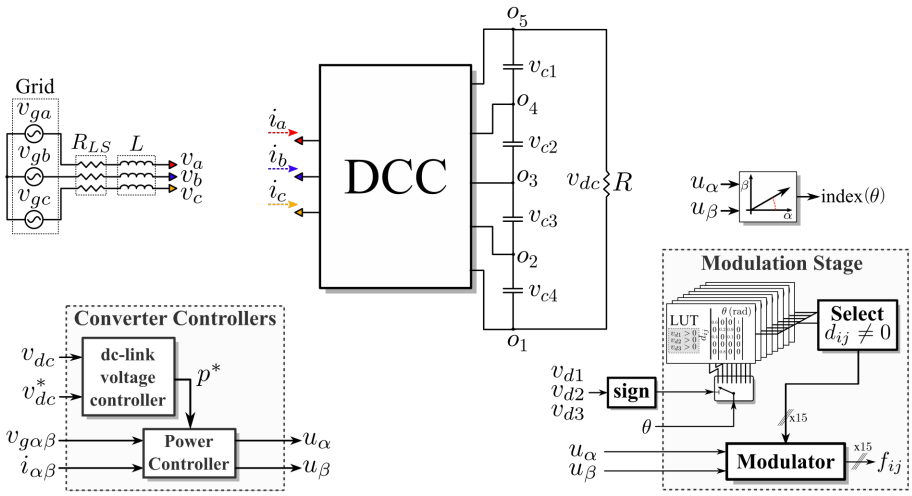

Figure 2.40 Implementation and control scheme of the proposed approach.

Steady-state improvement

This approach may present an increased harmonic distortion in the grid current in steady state due to sudden changes of balancing criterion from one sampling instant to the next one. Indeed, when the error signals are close to zero, a change of their signs is likely to happen, and it would imply changing the lookup table among the eight entries, probably yielding to an abrupt change in the modulation criterion. This phenomenon is, by itself, acceptable, however, when it occurs several times consecutively, it distorts the grid current as additional commutations are introduced in each transition. Another aspect to take into account is that it is not necessary that the balancing error signals tend to zero but to remain close to zero. Therefore, a modification in the algorithm described above—referred as base algorithm from now on—is proposed. The modification—referred as enhanced algorithm—tries to avoid, in steady state, frequent changes of balancing criterion.

In the enhanced algorithm, the change of balancing criteria —change from one of the eight lookup tables to another— is limited to occur only when one of the error signals v_{dp} is large enough. Therefore, a threshold ν is defined in such a way that when the absolute values of the three v_{dp} are smaller than it, the active lookup table is not changed. Only when one of them exceeds ν, the lookup table is changed using the "normal" procedure exposed above. The larger the value of ν is, the lesser the times the change of criterion would occur, but larger values of v_{dp} would be allowed. As a result, the values of v_{dp}

Table 2.9 Control and System Parameters.

Parameter	Value	Parameter	Value
Grid freq., f_g	50 Hz	Samp. and swit. freq., f_s, f_{sw}	10 kHz
Grid volt., v_{gabc}	230 $\mathrm{V_{RMS}}$	Power factor	1
Filter Ind., L	2 mH	Prop. Pow. Cont., K_p (DPC)	$2e^{-7}$
dc-link cap., C	3300 μF	Int. Pow. Cont., K_i (DPC)	$2e^{-5}$
dc-link load, R	$120 \rightarrow 60\ \Omega$	Prop. Volt. Cont., K_p^{dc}	0.05
dc-link volt. ref., v_{dc}^*	$700 \rightarrow 800$ V	Int. Volt. Cont., K_i^{dc}	1
Enhanced band, ν	10 V	Samp. for LUT gen., N	100

will be enclosed inside a band of width 2ν around 0 at the same time that the grid current will present a better harmonic distortion. In the following, the base algorithm and the enhanced one will be compared by means of simulations with other approaches, and between themselves in experiments.

Simulation results

This section is devoted to present some simulation results carried out in MATLAB-Simulink® that compares the current optimization approach with some well-known approaches for five-level DCCs with balancing capabilities. The system under consideration is the same than the one presented in previous sections, i.e. a five-level DCC in rectifier configuration. The used simulation and control parameters are shown in Table 2.9, which includes the parameters considered for the LUTs generation. In this regards, $N = 100$ samples in a grid period were considered for each combination of signs of v_{dp}, which resulted on the resolution of 800 optimization problems. The time needed to solve such number of problems were around 20 secs.

Firstly, the LUTs are generated assuming steady-state conditions. The used controllers, either for the LUTs generation and the simulations, follow the general scheme of a cascaded control loop, with the outer loop being a PI controller (parameters K_p^{dc} and K_i^{dc}) in charge of regulating v_{dc} towards its reference, and the inner loop being the model-based DPC controller (shown in Sect. 2.3.3 with parameters K_p and K_i).

For the comparison, two approaches are considered from the literature with balancing capabilities [89, 134], in addition to the two approaches presented in Sect. 2.3.3. Paper [134] uses a modification of the well-known SVM and will be referred as space-vector based algorithm (SVBA), paper [89] uses the FCS-MPC to control a grid-connected NPC inverter, whereas the approaches presented in Sect. 2.3.3 will be referred as original integrated control and modulation (OICM), for the base proposal, and modified integrated control and modulation (MICM), for the further improvement. Notice that despite the FCS-MPC presented in [89] is designed for three-level converters, the cost function is modified in this section to be valid for five-level converters, similarly to [135]. Regarding FCS-MPC, as the switches can only occur at the sampling instants, three simulations are presented for different sampling frequencies (f_s): 10, 25 and 50 kHz.

The phase currents obtained from simulation for these approaches are depicted in Fig. 2.41, and the switching states in Fig. 2.42, both with $v_{dc}^* = 800\,V$ and $R = 60\,\Omega$. Notice that the lookup tables were designed for $v_{dc}^* = 700\,V$. Consequently, these results show

Table 2.10 THD value and number of commutations (variation in % respect to base algorithm).

Algorithm	THD		Number of commutations	
Base	4.63		645	
Enhanced	4.05	(-12%)	550	(-15 %)
SVBA [134]	7.01	(+51%)	935	(+45 %)
FCS-MPC [89] (10 kHz)	13.42	(+190%)	210	(-68 %)
FCS-MPC [89] (25 kHz)	5.10	(+10%)	540	(-16 %)
FCS-MPC [89] (50 kHz)	2.54	(-45%)	1100	(+70 %)
OICM [119]	5.40	(+16 %)	1600	(+148%)
MICM [119]	4.20	(-9 %)	1333	(+106%)

that this approach is also valid for some operating point that were not considered in the design. The resulting current THD values and number of commutations in a grid period are shown in Table 2.10, where their variation in % with regard to the base algorithm presented in this paper are also highlighted. Notice how the proposed base and enhanced algorithms exhibit lower current distortion and lower number of commutations than SVBA and OICM. On the contrary, MICM achieves slightly better current distortion than the base algorithm at the cost of much larger number of commutations. In terms of the FCS-MPC approach, higher frequencies usually result in less current distortion, larger number of commutations and more demanding computational burden. It can be seen that FCS-MPC with the same f_s than the base algorithm yields unacceptable current distortion (13.42 %). In order to achieve a more feasible current distortion, the sampling rate has to be increased from 10 kHz to 25 kHz, for which the currents reach a THD value of 5.1 %, which is closer to the value of the base algorithm (4.63 %). At the same time, the number of commutations is increased proportionally to the sampling rate—again, this is true as long as the weights in the cost function of FCS-MPC are not changed—, which, for 25kHz, reaches a similar number of commutations than the enhanced algorithm (540 vs 550). Larger sampling rates (50 kHz) further reduce the current distortion (2.54 %) and increase the commutations (1100). In summary, in terms of current distortion and number of commutations, the base and enhanced algorithms exhibit a better behaviour than SVBA [134] and the previously presented OICM with $f_s = 10$ kHz, while FCS-MPC [89] has to appeal larger sampling rates to achieve similar performance. It is worth to mention that FCS-MPC uses a cost function whose weights can be modified as a tradeoff between current distortion, capacitor voltage balance and number of commutations. These simulations were carried out using the weights that achieve the capacitor voltage differences to be less than ν in steady state. Alternatively, MICM improves the current distortion when compared with the base algorithm (4.2 % vs 4.63 %) at the cost of yielding twice the number of commutations. Nonetheless, the proposed enhanced algorithm further improves the base algorithm performance achieving lower distortion and commutations than MICM.

As it has been mentioned, the improvement in the current distortion and number of commutations for the enhanced algorithm is due to the relaxation in steady state of the capacitor voltage balance criterion, as they are not forced to go to zero but to keep around

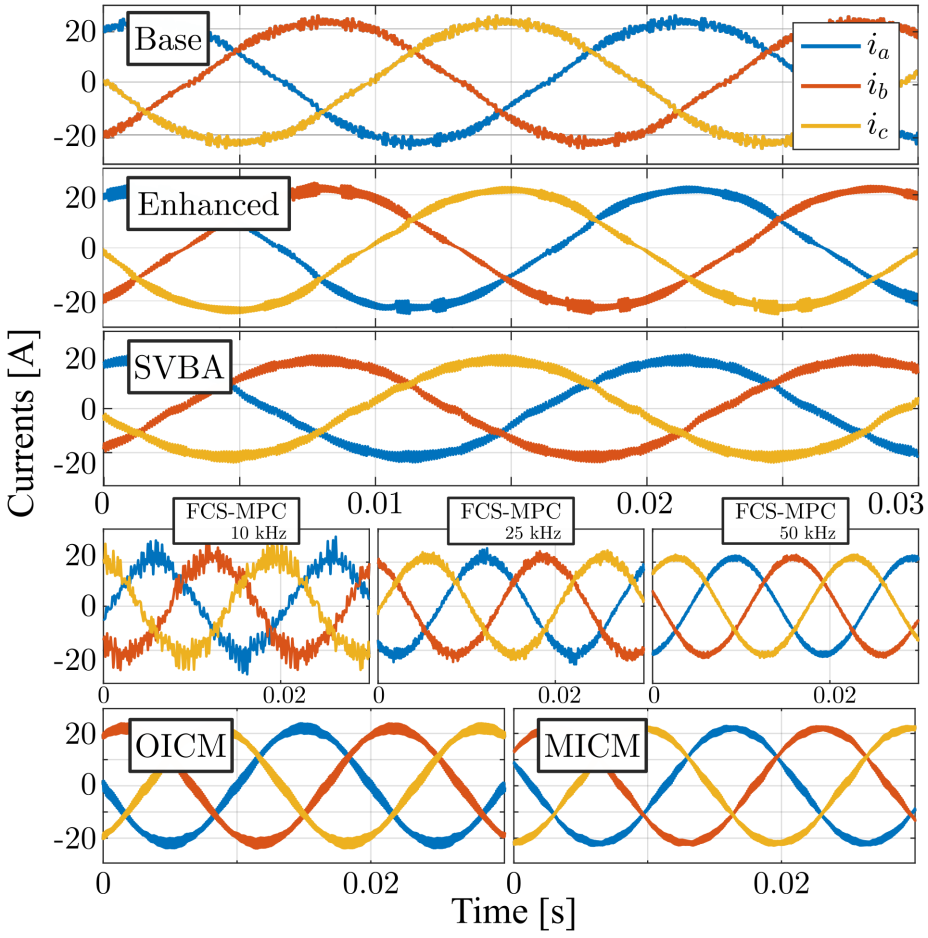

Figure 2.41 Three-phase currents in steady state when $R = 60\,\Omega$ and $v_{dc}^{*} = 800\,V$ for the base algorithm (top), the enhanced one (2^{nd}), the SVBA [134] (3^{rd}), the FCS-MPC [89] (4^{th}) considering three sampling rates (10, 25 and 50 kHz), and the OICM and MICM (bottom). The THD values of these currents are shown in Table 2.10.

a band of value ν. In this way, the change of balancing criterion—the selected lookup table (LUT) among the available 8— is done much less frequently as it can be seen in Fig. 2.42.

Regarding voltage balancing capabilities, a simulation starting from an unbalanced situation is depicted in Fig. 2.43 ($v_{d1} = -40$, $v_{d2} = 60$, $v_{d3} = -5$). At $t = 1\,s$, the balancing strategy for every approach is enabled showing the evolution of the capacitor voltages. The FCS-MPC algorithm exhibits the fastest performance but, because of the initial large values of $\{v_{d1}, v_{d2}, v_{d3}\}$, the current tracking is not prioritized in the cost function until these values are low enough. Therefore, there exists a transient where

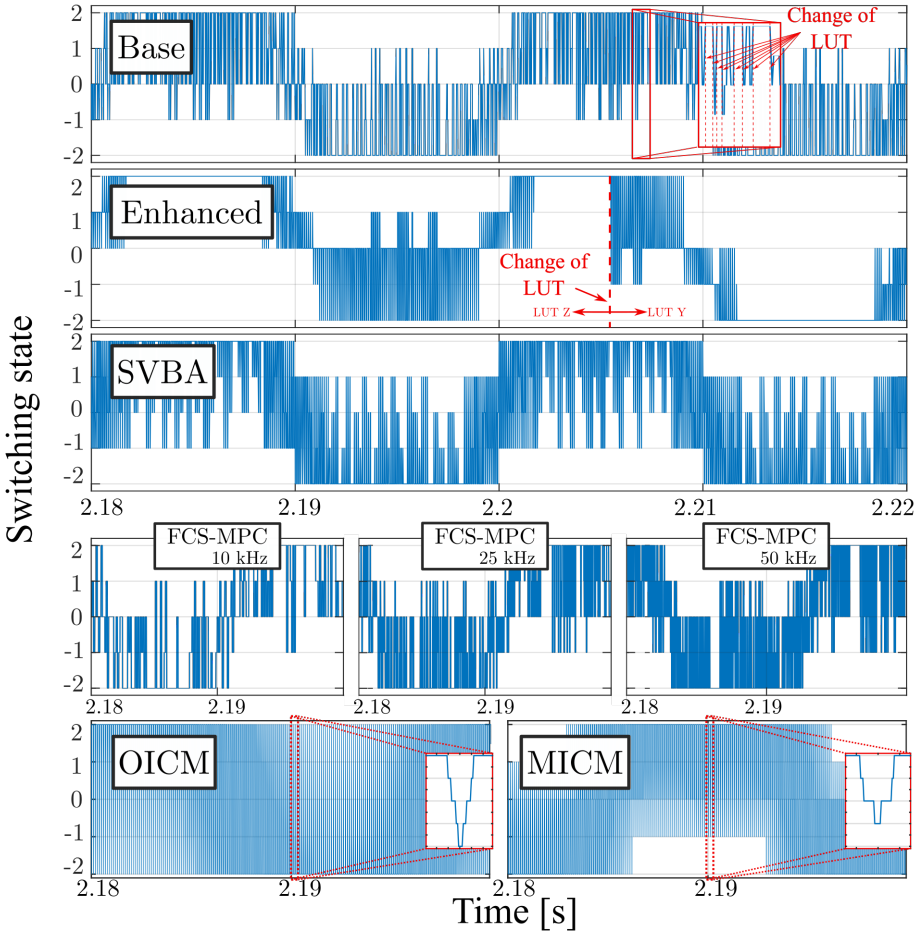

Figure 2.42 Switching state of phase a of the converter output with $v_{dc}^{*} = 800\,V$ and $R = 60\,\Omega$, for the base algorithm (1st), the enhanced one (2nd), the SVBA [134] (3rd), the FCS-MPC [89] (4th) considering three sampling rates (10, 25 and 50 kHz), and the OICM and MICM (bottom). The number of commutations for each approach is shown in Table 2.10.

the current tracking is affected. Besides, due to the same reason, there exist nonzero steady-state errors in the capacitor voltage balancing that depend on the cost function weights considered for the balancing task. Additionally, the larger the sampling frequency, the faster the balancing. The SVBA algorithm shows a slower balancing (around 500 ms to reach steady state) but reaching almost zero steady-state error. The OICM and MICM approaches have three capacitor voltage balancing control parameters (k_1,k_2,k_3 in Sect. 2.3.3) that determine the speed of the balancing. A higher value would yield a faster balancing response and lower steady-state error at the cost of a worse power tracking transients, similarly to the FCS-MPC. Nevertheless, these simulations used the

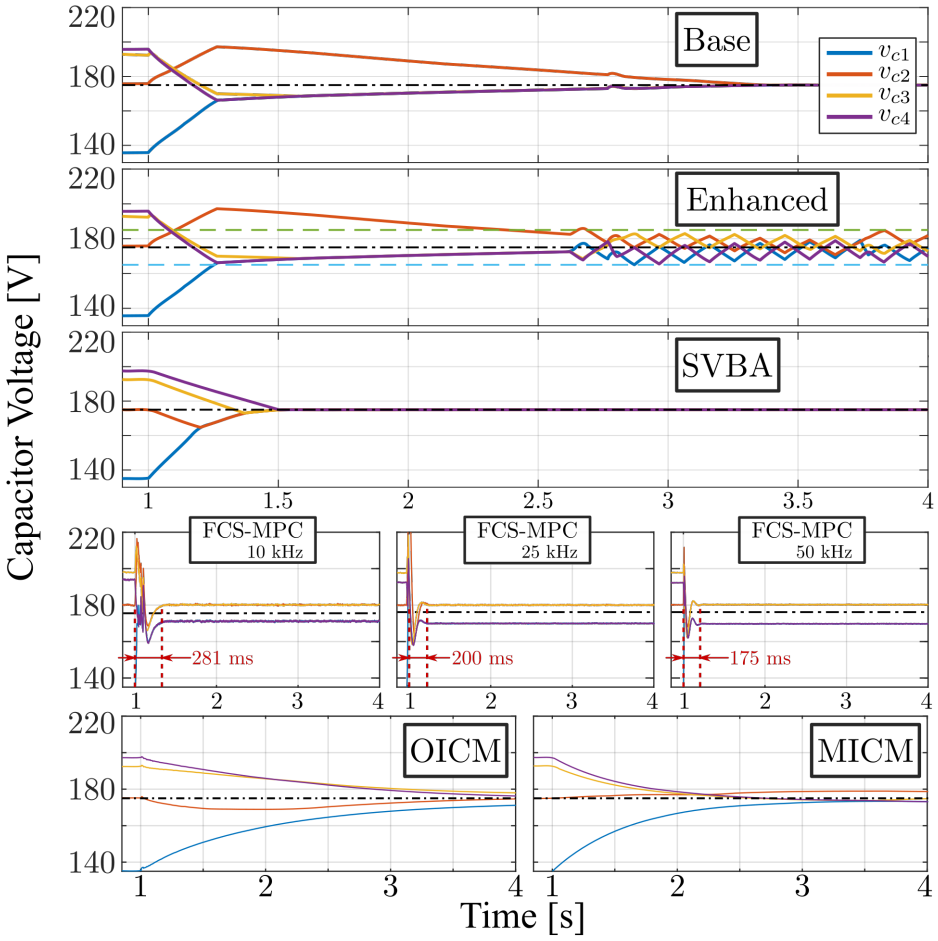

Figure 2.43 Capacitor voltages starting from an unbalanced condition ($v_{d1} = -40$, $v_{d2} = 60$ and $v_{d3} = -5$) for the base algorithm (1st), the enhanced one (2nd), the SVBA [134] (3rd), the FCS-MPC [89] (4th) considering three sampling rates (10, 25 and 50 kHz), and the OICM and MICM (bottom). The voltage balancing algorithms are switched on at $t = 1$. The voltage band and the desired value are depicted with dashed and semi-dotted lines respectively. $v_{dc}^{*} = 700\,V$ and $R = 120\Omega$.

same parameter value than the one used in 2.3.3 yielding the slowest balancing speed and non-zero steady-state error in the carried-out simulations. With regard to the proposed algorithms, the base and enhanced approaches present a voltage balancing that takes around two seconds to reach steady state (faster than OICM or MICM, but slower than SVBA or FCS-MPC). Comparing the base and the enhanced approaches, they result in similar balancing capabilities—indeed, its behaviour is the same whenever any capacitor voltage error signal is outside the band ν. The difference between them lies in their behaviour at

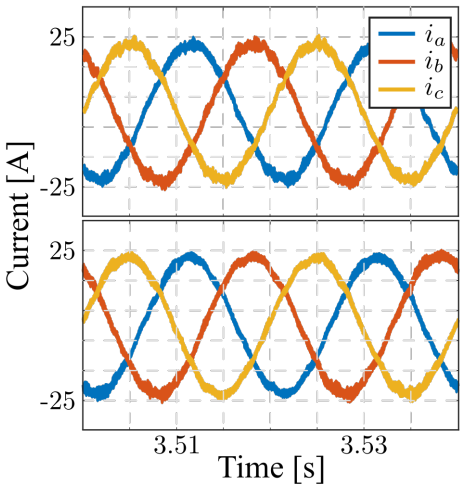

Figure 2.44 Experimental result: Three-phase currents in steady state for the base (top) and the enhanced (bottom) algorithms.

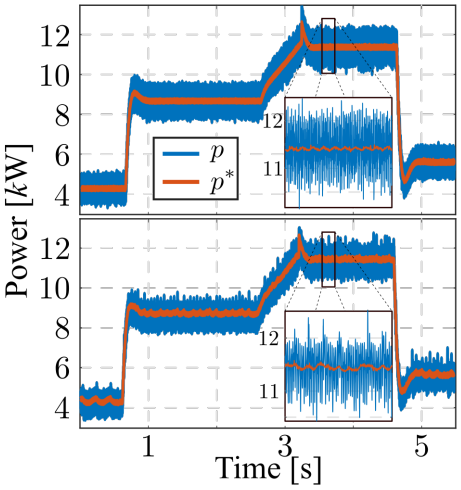

Figure 2.45 Experimental result: Power behaviour during the experiment for the base (top) and the enhanced (bottom) algorithms.

steady state. Because of the relaxation of the balancing objective, the enhanced algorithm avoids unnecessary changes in the evolution of the capacitor voltages (by avoiding selecting another lookup table) provided that the voltage balance signal errors are inside the band—depicted in dashed lines in Fig. 2.43—, while the base one tries to keep them as close to zero as possible.

In summary, regarding capacitor voltage balance, the exhibited approaches in this section are slower than FCS-MPC and SVBA but faster than OICM and MICM. Besides, the base algorithm reaches small steady-state error similar to SVBA. On the contrary, the enhanced algorithm keeps the errors moving inside a band (whose amplitude is a design parameter), while FCS-MPC, OICM and MICM yield some fixed error in steady state. Nevertheless, the voltage balance is a secondary problem, while low current distortion and low losses (proportional to the number of commutations) are more important. In numerous applications this slowness is a reasonable price to pay in order to obtain the good results shown in Table 2.10.

Experimental results

This section is devoted to confirm the validity of the proposed approaches. For this, experimental results are obtained using the same equipment shown in previous sections (Fig. 2.21 in Sect. 2.3.3) with the same parameters than the previous simulation section (Table 2.10). Figure 2.44 depicts the behaviour of the phase currents in the experiment in steady-state ($v_{dc} = 800\,V$ and $R = 60\,\Omega$) for the base and the enhanced algorithm. Accordingly, the harmonic spectrum and the THD value of these currents are also depicted in Fig. 2.46, validating the improvement for the enhanced algorithm in terms of current distortion at steady state.

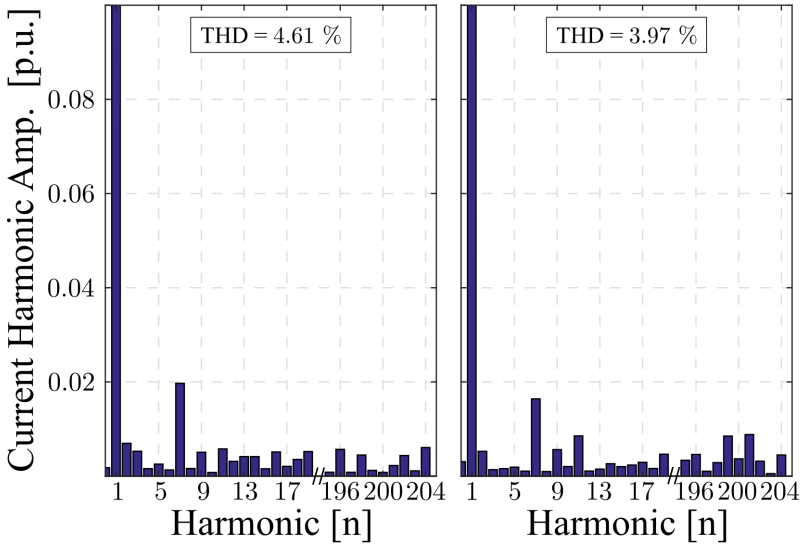

Figure 2.46 Experimental result: Harmonic spectrum of phase currents (Fig. 2.44) for the base (left) and the enhanced (right) algorithms.

In order to test the behaviour of the system under different conditions, for which the lookup tables were not designed, an abrupt change in the load from 120 to $60\,\Omega$ at $t = 0.7$ s, a smooth change in v_{dc}^* from $700\,V$ to $800\,V$ starting at $t = 2.6$, and the load returning to $120\,\Omega$ from $60\,\Omega$ at $t = 4.6$ s are considered. The smooth change in v_{dc}^* consists of a linear ramp with a duration of $0.7\,s$. These changes can be seen in Fig. 2.45 where the evolution of the active power is depicted. The capacitor voltage evolution during this test are also shown in Fig. 2.47, where the capacitor voltages follow the capacitor voltage reference v_{dc}^* properly. Note that this latter figure exhibits a noticeable difference between the base and the enhanced algorithm, as the enhanced algorithm makes the capacitor voltages to stay within a band around the reference instead of being tightly attached to it. Let us also remark that the latter feature affects only the capacitor voltage balancing loop, given that the addition of the four capacitors should match v_{dc}^* as it is dictated by the outer and inner controllers.

Lastly, and similarly to the simulation section, the capacitors voltage evolution starting from an unbalanced situation—the one considered in simulations—are shown in Fig. 2.48 for the base and the enhanced algorithm, where the band in which the signals move at steady state can also be seen. Despite the fact they do not tend to zero for the enhanced algorithm, their resultant ripple are affordable as they are comparatively small. All these figures corroborate the simulation results and the good performance of the proposed method.

Conclusions and future lines of research

In contrast to the integrated control and modulation algorithm, this proposal considers the common approach of separating the modulation stage from the controller. From this, the modulation stage is formulated as a linear, mixed-integer optimization problem with

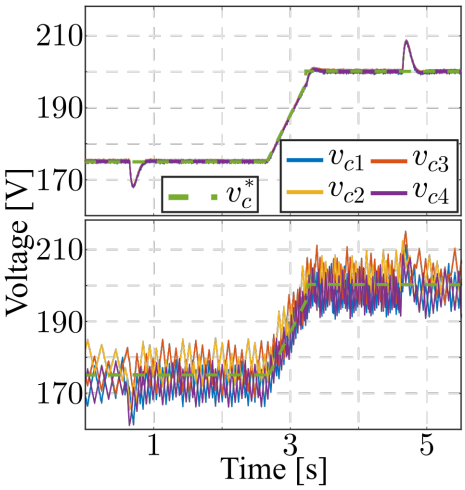

Figure 2.47 Experimental result: Evolution of the capacitor voltages in addition to their reference $v_c^* = v_{dc}^*/4$ during the experiment for the base (top) and the enhanced (bottom) algorithms.

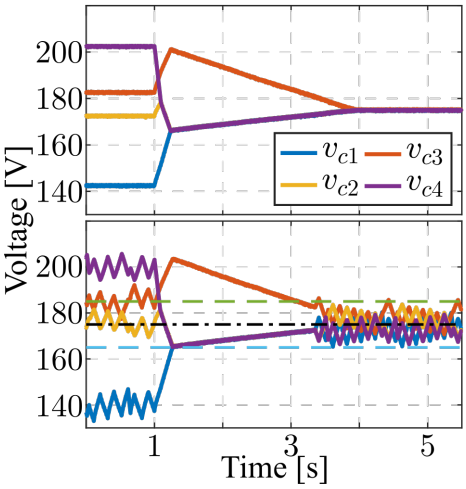

Figure 2.48 Experimental result: Evolution of the capacitor voltages starting from an unbalanced condition for the base (top) and the enhanced (bottom) algorithms. Band and equalized value depicted with dashed and semi-dotted lines respectively. $v_{dc}^* = 700\,V$ and $R = 60\,\Omega$.

constraints in such a way that the capacitor voltage balance has to be tackled along with the implementation of the input control signals, similarly to the standard modulators. Thanks to the optimization formulation, the number of commutations is minimized exploiting the remaining degrees of freedom after the voltage and power control has been implemented. The optimization problem is costly to be solved online, and thus, several lookup tables are used. For this, a procedure for adequately use the lookup tables is given including a relaxation of the algorithm in steady state in order to improve the harmonic distortion. The resulting approach is tested in both simulations and experiments showing the good behaviour of the proposed method under some changes in the load and the desired dc-link voltage, showing some flexibility in the operation point and robustness to load variations.

A future line of research that will be covered in the next section is the extension of this approach to those cases where larger variations of the operating conditions are present, such as different power factor conditions or modulation indexes. Alternatively, considering the duty ratios implemented in the previous switching period into the optimization problem of the actual switching period is left as a possible line of research, as this factor has not been considered in the cost function. In fact, this effect is indirectly taken into account in the enhanced implementation of the LUT. However, its inclusion in the optimization problem could potentially derive in an improved algorithm.

2.3.7 Pseudo-optimal modulation based on machine learning

Despite the fact that the previous proposal was validated by means of simulation and experiments, even with variations on the operating point, the LUTs depend on the considered conditions under which they were generated. Due to this, it is predictable that large variations of the operating point make the modulation to fail in fulfilling the control objectives. Thanks to the proposed implementation procedure, the power control is always fulfilled and the duty ratio saturation is avoided, but the capacitor voltage balance may be not be addressed. Indeed, changes in the desired power factor value—by means of the reactive power—shift the current with respect to the grid voltage, which makes the balancing dynamics—dictated by the injected current into the different levels—to behave unsatisfactorily. For this, due to the complexity of solving the optimization problem, additional LUTs would be required to cover those operating points with different power factor values, which could make the implementation procedure very complex and with a large computational burden.

This is the main issue that the contribution exhibited in this section and presented in [120] tries to cover. The optimization problem is solved offline for several operating conditions, including some with different power factor values. Then, the results are gathered into a dataset to train classification and regression trees (CART) that are later used during online operation. With this, it is expected—and later proved by experiments and simulations—that the generalization capability of the CARTs allows a more flexible and less resource-intensive implementation, which is capable of operating at points outside the considered ones in the training dataset. In contrast to the LUT-based implementation, this proposal generates eight CART diagrams—one for every combination of the signs of v_{d1},v_{d2},v_{d3}—which dictates the modulation performance similarly to the previous approach. In addition to this contribution, the optimization problem is revisited and some modifications are introduced in the optimization problem formulation with the aim of improving the steady-state results.

Machine learning

The increase in processing power and refinement of data science algorithms have boosted the use of machine learning for almost all sectors in the industry. Power electronics is not an exception in this regard, and some proposals have been developed for microgrids [136] or DC-DC converters [137]. In terms of machine learning, two categories are distinguished: supervised and unsupervised learning. Supervised learning takes place when the learning algorithm gets the input-output datasets, and it is suitable for optimal control by means of tuning network weights along with one or more performance indicators to be minimized. Unsupervised learning, in contrast, is used for classification algorithms that require no feedback, and hence it is less common for optimization and controlling purposes.

CART generation is a well-known supervised classification algorithm that can make explicit the critical features involved in a classification process. Besides, its easiness of implementation, nonparametric modelling and nonlinear classification capability make it an appealing strategy to be considered for the multilevel power converter modulation issue. In fact, choosing which levels to use for every phase and sampling instant can be seen as a classification problem. For this, the CART algorithm is well suited to tackle the problem

considered, that is, to summarize the information obtained from the optimization problem into easily-implementable decision trees that preserve the optimality of the switching sequence, while a general solution is obtained for a wider range of operating points.

Modified optimization problem formulation

The mixed linear-integer optimization problem formulation described in [132] and presented in the previous section [117] is initially considered. Again, the optimization problem results in the values of the duty ratios d_{ij} that accomplish the fulfillment of the current or power control (referred as the fulfillment of u_α and u_β in accordance to (2.130)–(2.131)), and the capacitor voltage balance (making $v_{dp}\frac{dv_{dp}}{dt} \leq 0$ for $p = 1,2,3$), while the minimization of the number of commutations is pursued.

From the previous section, the cost function (2.136) can be initially considered:

$$f_{\text{cost}} = \sum_{i=a,b,c} \left(\sum_{j=1}^{5} s_{ij} + \sum_{m=1}^{6} p_{im} q_{im} \right) \tag{2.137}$$

with the following constrains

$$s_{ij} - d_{ij} \geq 0 \tag{2.138}$$

$$s_{ij_{m1}} + s_{ij_{m2}} - r_{im} \leq 1 \tag{2.139}$$

$$r_{im} - p_{im} - \sum_{j=j_{m1}+1}^{j_{m2}-1} s_{ij} \leq 0 \tag{2.140}$$

for $i = a,b,c$, $j, j_{m1} < j_{m2} \in [1,5]$ and $m \in [1,6]$. The meaning of these variables were described in the previous section (Sect. 2.3.6). In the following, some improvements are added with respect to the previous problem formulation. These improvements come from considering that the previous objectives are included in the cost function as integer numbers, and thus different optimal candidates could result in the same score. In these cases, those solutions that achieve the fulfillment of the strict inequality $v_{dp}\frac{dv_{dp}}{dt} < 0$ should be prioritized. Additionally, the magnitude of the derivative of v_{dp} may also be taken into account in order to accelerate the v_{dp} convergence towards zero. For this, the following modified cost function is proposed

$$f_{\text{cost}}^{\text{mod}} = f_{\text{cost}} + \sum_{p=1}^{3} \left(\alpha h_p - \alpha_1 \text{sign}(v_{dp}) \frac{dv_{dp}}{dt} \right), \tag{2.141}$$

with h_p being a positive integer and with the following added constraint

$$h_p - \frac{dv_{dp}}{dt}\text{sign}(v_{dp}) > 0, \quad h_p \geq 0, \quad \text{for } p = 1,2,3 \tag{2.142}$$

which results in $h_p = 0$ if $\frac{dv_{dp}}{dt}\text{sign}(v_{dp}) < 0$ and $h_p > 0$ otherwise. Additionally, α_1 and α are the weighting factors to fix the contribution of the magnitude error signals derivative

and h_p variable, respectively. Considering that the balancing of all capacitors should prioritize the convergence speed of the error signals, these weighting factors are selected such that $\alpha_1 \ll \alpha$. Besides, this added term should only be taken into account to select the optimal solution when the original cost function shows no difference between two candidates, and therefore $\alpha_1 \ll \alpha \ll 1$. Considering that sign$(v_{dp})$ is known beforehand, the cost function and all the constraints are still linear, and thus the optimization problem is still linear, mixed-integer.

Optimization problem solution

Again, the optimization problem must be solved offline due to its large computational burden. For this, the steady-state behaviour of the system under nominal conditions is simulated over a grid period, and N samples are stored for the state variables of the system. The steady-state and nominal conditions involve the following assumptions

1. Sinusoidal phase currents and grid voltages.
2. Dc-link voltage and reactive power equal to their references.
3. Active power equal to the one demanded by the resistive load attached to the dc-link.
4. Capacitor voltages perfectly balanced.

The simulation considers the averaged model of the system, which gives the unitary value of the phase currents and the value of the control signals u_α, u_β for every sample. Using this information, the optimization problem is solved and the corresponding duty ratios are obtained. Given that the optimization resolution requires the knowledge of the values of sign(v_{dp}), they are assumed beforehand, resulting in eight possible scenarios for every simulation. Note that, following this procedure, the results obtained are associated with one value of dc-link voltage reference and reactive reference. The previous proposed approach was to store these results in eight LUTs to be used later during online operation. Despite the fact that it proved to give good results for the nominal conditions, large variations of the reactive power makes the balancing error signal to diverge from zero. For this, it is proposed to simulate several conditions of dc-link voltage and reactive power references, to solve the optimization problem for every sample and gather the results in eight different datasets.

Similarly to the previous approach, it is noticed that the solution usually has one duty ratio equal to 1, i.e. the corresponding phase is fixed to that level and it does not use any other level, while the remaining phases have only two duty ratios different from zero. Consequently, it is assumed that the adopted solution will follow this principle: One phase fixed to one level, and two phases commuting between two levels each. In order to achieve generality, each result is coded into a variable that takes this principle into account, and it is stored in the previous datasets. The CART algorithm is later trained with these datasets being the coded result the output of such CART. The following subsection will provide more information about the coding of the CART inputs and the results. Fig. 2.49 shows the scheme of the training process. The resultant algorithm (the classification trees) can be implemented online, and given that several operating points are considered, a wide range of operating points is expected to be covered as it will be shown in the simulation and experimental sections.

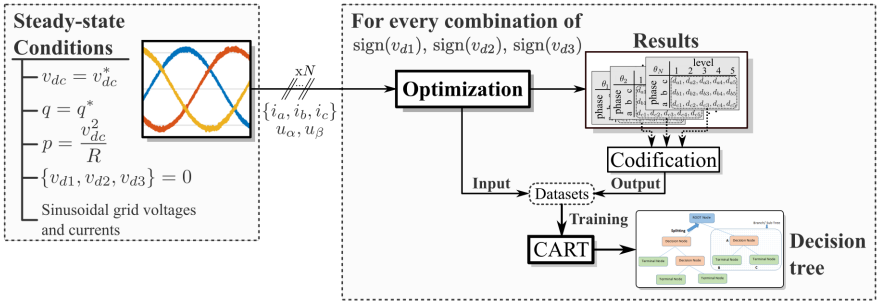

Figure 2.49 Flowchart of the carried out steps to obtain the decision trees based on the optimization problem.

CART algorithm

As depicted in Fig. 2.49, the input data should represent the potential values of the currents and control signals, and therefore, it is convenient to codify these information in a qualitative manner aiming for generality. Additionally, in order to synthesize the CART output information, the result is coded following a simple rule that is exhibited in this section.

Input data for the CART algorithm

Considering the grid voltage and current nature and, in order to establish a more generic training dataset for the CART, some qualitative information has to be extracted from them. The qualitative criteria was based on expert knowledge and the analysis of the optimization results for several test cases. Regarding the potential values of the homopolar component x, Eq. (2.131) is recalled, where its limits can be derived by knowing that $u_i \in [-2,2]$. Therefore, these limits are defined and referred as $x_{\min} = -2 - \min(\eta_a,\eta_b,\eta_c)$ and $x_{\max} = 2 - \max(\eta_a,\eta_b,\eta_c)$. The considered qualitative data are defined as follows

- The sign of the currents i_a, i_b, i_c: -1 for negative values, and 1 for positive values. (3 values)
- An integer number for each phase $i = a,b,c$ (level_i) that indicates between which two levels the associated voltage reference η_i is found (obtained from the reverse Clarke transformation of u_α and u_β for $x = 0$). The code for this number is shown in Table 2.11. (3 values)
- A code (r) that indicates the order relation among i_a, i_b and i_c. This code is shown in Table 2.12. (1 value)
- Variables y_{ij} for $i = a,b,c$ and $j = 1,2,\ldots,5$ are set to 1 when there exists a value of x fulfilling $x_{\min} \leq x \leq x_{\max}$ such that the corresponding value of $\eta_i + x$ is equal to j. This means that, for the current sample data, it is possible to consider a value of the homopolar component x such that u_i is equal to level j, while $u_i \in [-2,2]$ for $i = a,b,c$. Therefore, $y_{ij} = 1$ if $x_{\min} \leq j - 3 - \eta_i \leq x_{\max}$, and $y_{ij} = 0$ otherwise. (15 values).

Table 2.11 Integer number to indicate associated levels for η_i.

level$_i$	η_i	level$_i$	η_i
1	[-2,-1]	3	(0,1]
2	(-1,0]	4	(1,2)

Table 2.12 Integer number to indicate current order.

r	Current order	r	Current order
1	$i_a \geq i_b \geq i_c$	4	$i_c \geq i_b \geq i_a$
2	$i_a \geq i_c \geq i_b$	5	$i_b \geq i_c \geq i_a$
3	$i_c \geq i_a \geq i_b$	6	$i_b \geq i_a \geq i_c$

Table 2.13 Integer number a_1 to indicate which d_{ij} equals one.

a_1	(i,j)	a_1	(i,j)	a_1	(i,j)	a_1	(i,j)	a_1	(i,j)
1	(a,1)	2	(a,2)	3	(a,3)	4	(a,4)	5	(a,5)
6	(b,1)	7	(b,2)	8	(b,3)	9	(b,4)	10	(b,5)
11	(c,1)	12	(c,2)	13	(c,3)	14	(c,4)	15	(c,5)

Table 2.14 Integer number a_2/a_3 to indicate pair of used levels.

code	levels	code	levels	code	levels
1	$1-2$	5	$1-3$	8	$1-4$
2	$2-3$	6	$2-4$	9	$2-5$
3	$3-4$	7	$3-5$	10	$1-5$
4	$4-5$				

Output data for the CART algorithm

The decision tree output is coded assuming that the optimization problem resolution will have one phase fixed at one level, while the other two phases commute between two different levels. Among the obtained results of the optimization problem, few of them did not follow this distribution, and therefore, they were not included in the training dataset. A code that captures the assumed information is defined by using three variables a_1, a_2, a_3:

- Variable a_1 indicates the pair of values i and j such that $d_{ij} = 1$, i.e. the phase i that is fixed at level j. These values are shown in Table 2.13 covering 15 possible values.
- The other two phases only commute between 2 levels. Consequently, a_2 and a_3 indicates these pair of levels for each phase. The correspondence of a_2 and a_3 with the phases follows alphabetical order: for example, if the phase represented with variable a_1 is phase b, code a_2 corresponds to phase a and code a_3 to phase c. The pairs are coded by enumeration as shown in Table 2.14. As a result, variables a_2 and a_3 cover 10 combinations each.

Considering the combination of the three variables into one, $15 \times 10 \times 10 = 1500$ possible values are obtained. This variable, referred as output code, is used as the output for the CART algorithm and it is computed as follows

$$\text{Output code} : (a_1 - 1) \cdot 10^2 + (a_2 - 1) \cdot 10 + a_3 - 1, \tag{2.143}$$

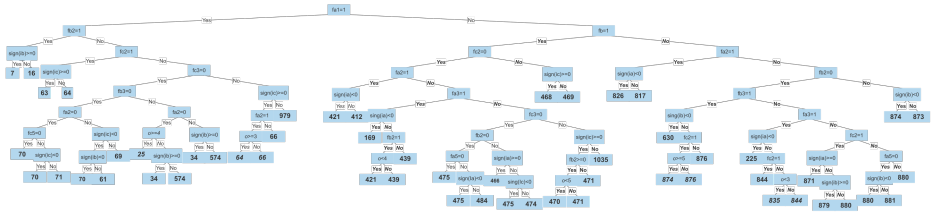

Figure 2.50 Example of a decision tree obtained for $v_{d1} > 0, v_{d2} > 0, v_{d3} > 0$ with the output shown in bold.

which represents an unique combination of the three integer variables.

Decision trees generation

The trees are generated using the *recursive partitioning and regression trees* technique from the *rpart* library for R language. The arguments of this function are: the input-output variables defined previously; the classification method, which is set as "class"; the way the decisions are considered, in this case, through the complexity parameter cp, which determines that a split is not carried out if it does not decrease the overall lack of coverage by the value of cp; and a vector of cost values. The latter vector contains one cost value for each considered input in such a way that the inputs with larger cost values associated would appear less frequently in the decision tree. The value of cp is tuned in such a way that a minimum of 85 % of coverage of the training data set is obtained for every decision tree.

In summary, there exist 22 variables to be used as input parameters and one coded integer result whose value could range from 1 to 1500. Gathering all these information for every combination of sign(v_{dp}) into one dataset for all samples within one grid period, the CART algorithm can be trained, and a decision tree is obtained as a result. As an example, the generated tree for the three positive signs of v_{dp} is depicted in Fig. 2.50, where it can be seen that a maximum of nine comparisons are needed in each execution of the tree, which is an easy and fast task for real-time implementation purposes.

Decision trees implementation

Once the decision trees are obtained, they can be easily implemented into the corresponding control system by means of nested "if...else" statements. During online operation, the qualitative information used for the CART training is extracted from the measurements and control signals u_α and u_β, the combination of sign(v_{dp}) determines the corresponding decision tree and it is consulted with this information, resulting in the output code. Then, the following procedure is carried out for the modulation stage

1. Variables a_1, a_2 and a_3 are obtained from the output code. To depict an example of the decoding process, let us consider an output code of 574 from Fig. 2.50, then variables a_1, a_2, a_3 are extracted by means of simple integer division as follows

$$a_1 = \text{floor}(\text{code}/10^2) + 1 = 6 \tag{2.144}$$

$$a_2 = \text{floor}((\text{code} - a_3 \cdot 10^2)/10) + 1 = 8 \tag{2.145}$$

$$a_3 = \text{floor}((\text{code} - a_3 \cdot 10^2 - a_2 \cdot 10)) + 1 = 5 \tag{2.146}$$

where floor refers to the function that outputs the largest integer that is less than or equal to the input.

2. Using (2.131) and the information provided by a_1 (Table 2.13), i.e. which j and i should fulfill $d_{ij} = 1$, the value of x is obtained.
3. By knowing x and the information provided by a_2 and a_3, i.e. which pair of j values for each of the remaining phases should fulfill $d_{ij} \neq 0$, the remaining d_{ij} are computed. Note that, as it has been assumed that these phases commute using two levels, the determination of d_{ij} is unequivocal.

At this point, it could happen that the code obtained from the corresponding decision tree might not be implementable in the considered instant. This is the case when the u_α,u_β values cannot be represented using the levels indicated by a_1, a_2 and a_3. To cover this issue, the following implementation procedure is proposed:

1. The result is decoded and the levels to be used for each phase are obtained according to a_1, a_2 and a_3: phase fixed at one level will be referred as i_{fix} and the corresponding level as l_{fix}; and the other phases—referred as i_1 and i_2—are fixed at two different levels, each one referred as j_{11}, j_{12} and j_{21}, j_{22} respectively.
2. The indicated fixed phase (i_{fix}) should be accomplished at the specific level (l_{fix}), that is:

$$x_{\min} \leq \underbrace{l_{\text{fix}} - 3 - \eta_{i_{\text{fix}}}}_{x_{\text{fix}}} \leq x_{\max}. \tag{2.147}$$

If this can be accomplished, then $x = x_{\text{fix}}$, otherwise x is saturated to the closest value $x_{\min}$ or $x_{\max}$ such that it is still fixed at one level.

3. Phases i_1 and i_2 follows a similar idea. For each of them, they should be modulated using the indicated levels taking into account the previous value of x. This is feasible only if the following condition is fulfilled for each phase

$$j_{11} \leq \eta_{i_1} + 3 + x \leq j_{12} \tag{2.148}$$

$$j_{21} \leq \eta_{i_2} + 3 + x \leq j_{22}. \tag{2.149}$$

In the case the condition for the corresponding phase is not fulfilled, the used levels for that phase are modified to the nearest ones, that is the closest integer values above and below of $(\eta_i + 3 + x)$.

Thanks to this procedure, a more robust implementation is given that prioritizes the constraints associated with u_α and u_β (2.131). This implementation scheme is depicted in Fig. 2.51.

Despite the fact that the previous procedure aims for a robust implementation, the obtained duty ratios might not be the optimal values according to the formulated problem, which is the reason why this proposal is referred as pseudo-optimal modulation. Besides,

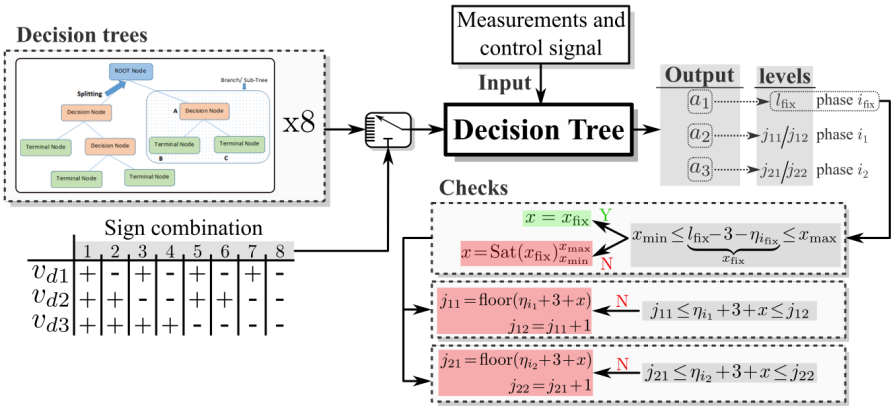

Figure 2.51 Implementation scheme to guarantee proper u_α, u_β modulation.

there are other potential sources of error that could make the implemented result to diverge from the optimal one:

1. The measured variables, as well as the values of u_α and u_β, may not correspond exactly to any of the training data sets, and therefore the result is inferred from the training datasets.
2. The CART algorithm has a coverage error and not all cases used for the training are correctly matched in the output given by the decision trees—The ones created for this work had a minimum coverage above 85 %.
3. Those cases that did not follow the generic rule of one phase fixed to one level and the others using only two levels were neglected from the dataset. Nevertheless, they represented less than 3 % of any of the solved optimization problem.

Despite this, simulation and experimental testing show satisfactory results, as it is shown in the following sections.

Simulation results

Similarly to the LUT-based approach, this proposal is compared in simulation with other modulation approaches in order to exhibit its main differences and similarities. For this, some simulations are carried out in MATLAB-Simulink® with the converter and control parameters shown in Table 2.15. Due to the fact that this proposal considers that the u_α and u_β values are already determined by an inner controller that is out of the aim of the considered objectives, the well-known nonideal PR controller is used [34] for this purpose, with the control parameters depicted in Table 2.15. Similarly, the outer controller in charge of regulating v_{dc} towards v_{dc}^* is considered to be an standard PI controller. The parameters that are required for the CART generation and training are also shown in Table 2.15.

The operating points considered in the generation of the training dataset are shown in Table 2.16. Lastly, the cost values considered for the CART training algorithm are selected and justified as follows

Table 2.15 Converter Parameters.

Parameter	Value	Parameter	Value
Grid freq., f	50 Hz	Sampling freq., f_s	10 kHz
Grid voltage, v_{gabc}	230 V_{RMS}	Switching freq., f_{sw}	10 kHz
Inductance, L	2 mH	Prop. gain PR, k_p	5
Capacitance, C	3300 μF	Resonant gain PR, k_r	200
dc-link load, R	$[60, \text{inf}]$ Ω	Prop. gain dc-link, K_p^{dc}	0.05
dc-link voltage reference, v_{dc}^*	$[700, 800]$ V	Integral gain dc-link, K_i^{dc}	1
Samples for optimization, N	100	LPF cut-off freq. (PR), ω_c	$2\pi 5$ rad/s
Opt. weighting factor, α_1	0.01	Resonant freq. (PR), ω_r	$2\pi 50$ rad/s
Opt. weighting factor, α	0.001	CART complex param., cp	0.002

Table 2.16 Operations points considered for the training data set.

nº	v_{dc} (V)	p (kW)	q (kVA)	nº	v_{dc} (V)	p (kW)	q (kVA)
1	800	10	0	2	800	0	10
3	800	0	-10	4	700	10	0
5	700	0	10	6	700	0	-10

- The sign of the currents and their order code (r) keep the same value for a large number of samples within one grid period, and thus they should be consulted less frequently: Cost value $= 5$
- Variables level$_i$ are the next considered as they change more frequently: Cost value $= 2.5$
- Variables y_{ij} are the easiest to classify due to their binary nature, and they also provide useful information about the feasible values of x: Cost value $= 1$.

As it was mentioned previously, the larger the cost value assigned to an input, the less frequently they are included in the decision tree.

The five additional modulation methods for five-level DCC converters that are simulated in this section, apart from the proposed one (referred as CART), are the following ones: the original proposal of the optimization problem implemented through a look-up table exhibited in the previous section and presented in [117] (LUT), a space-vector based algorithm (SVBA) [134], a model-predictive control based on finite control set (FCS-MPC) [89], and the two integrated control and modulation methods proposed previously exhibited and extracted from [116] (OICM and MICM). As it was mentioned in Sect. 2.3.6, the FCS-MPC approach requires larger switching frequencies to achieve a similar switching performance than those PWM-based approaches, as the switching may only take place at those instants. Therefore, three sampling and switching times are considered for the FCS-MPC: 10, 25 and 50 kHz, similarly to the previous section. See the simulation section (Sect. 2.3.6) of the previous approach for a brief explanation of each one of these approaches.

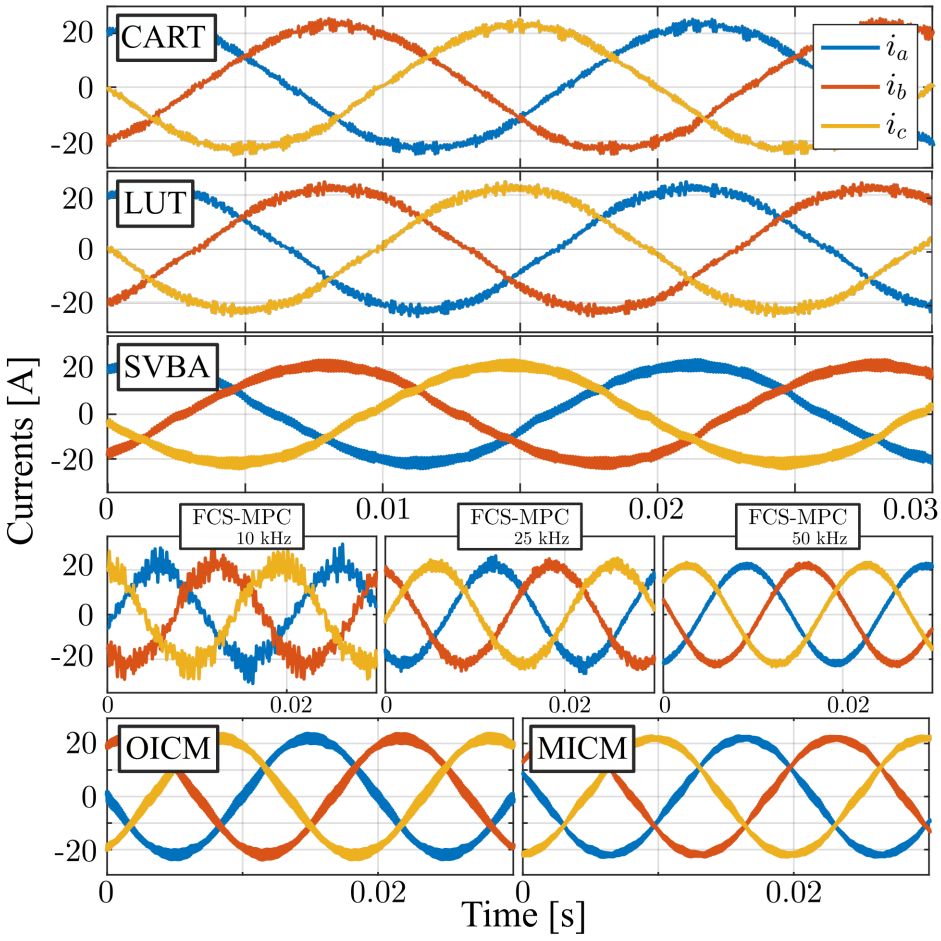

Figure 2.52 Three phase currents at steady-state conditions of the approaches considered.

Firstly, the phase currents in steady state ($v_{dc} = 800$ V, $R = 60\,\Omega$, $q^* = 0k$VA) for each of the modulation methods are depicted in Fig. 2.52. Similarly, the switching output of each of them under the same conditions are depicted in Fig. 2.53. For ease of comparison, the performance indicators: total harmonic distortion (THD) and number of commutations over a grid period, extracted from these figures are shown in Table 2.17. As it is expected, the proposed method achieves similar current distortion value than the LUT-based method, given that both performs under the same optimization formulation, and the operating point is the one considered for the LUT obtention. In terms of number of commutations, the proposed method (CART) achieves a reduction in the number of commutations (550 vs 645). This could be explained from the generalization capability of the CART, which overrides the less frequent cases with another more frequent case when they have the same CART inputs and different outputs. Therefore, simulations show that CART implementation achieves a better performance in steady state compared

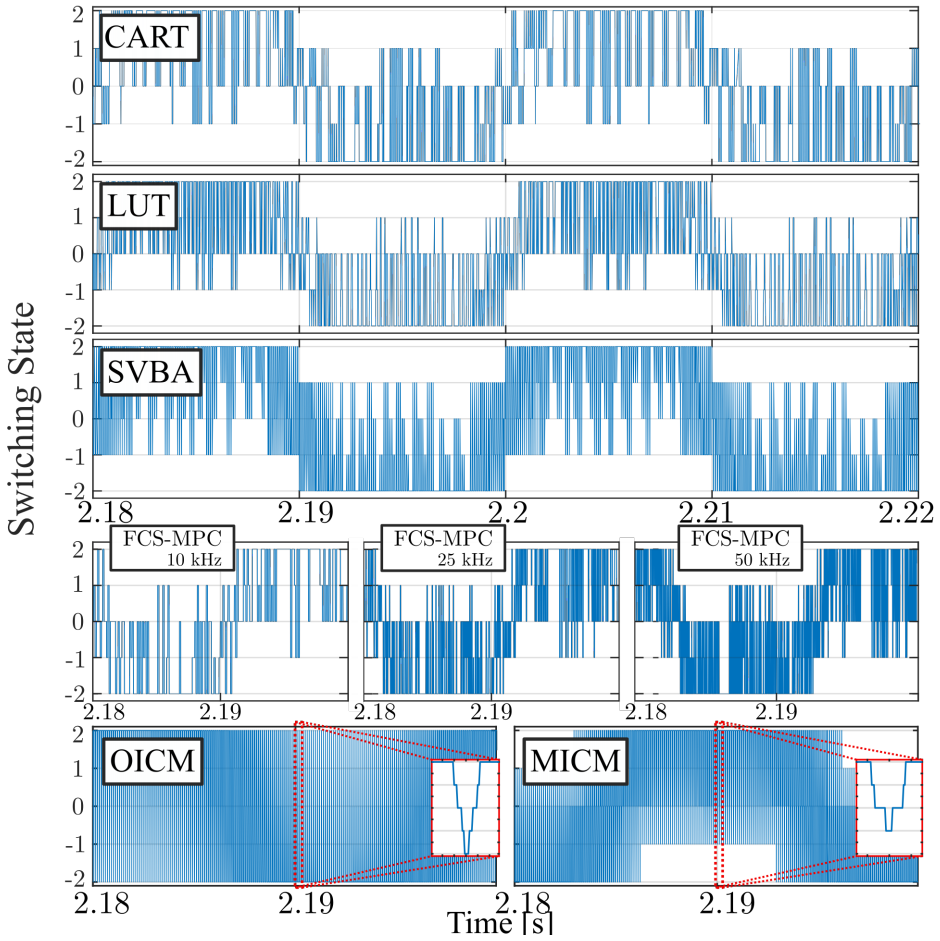

Figure 2.53 Switching state of phase a of the approaches considered.

to the LUT–based implementation, even under the conditions for which the LUT was implemented. In terms of comparison with the other approaches, CART implementation achieves better current distortion and lower number of commutations than OICM and SVBA. Alternatively, MICM shows an improvement in the current distortion at the cost of yielding more than twice the number of commutations. Similarly, FCS-MPC requires to increase the sampling frequency to yield lower current distortion, which also comes at the cost of increasing the number of commutations. Nevertheless, at 25 kHz, FCS-MPC exhibits a similar number of commutations than CART (540 vs 550) but an increased current distortion.

Lastly, to depict the capacitor voltage balancing capabilities for the considered methods, Fig. 2.54 is depicted. This figure shows how the capacitor voltages evolve when the balancing start at $t = 1$ from an unbalanced voltage condition ($v_{d1} = -40, v_{d2} = 60, v_{d3} = -5$ for $t < 1$). To evaluate the flexibility of each approach, several tests has been performed

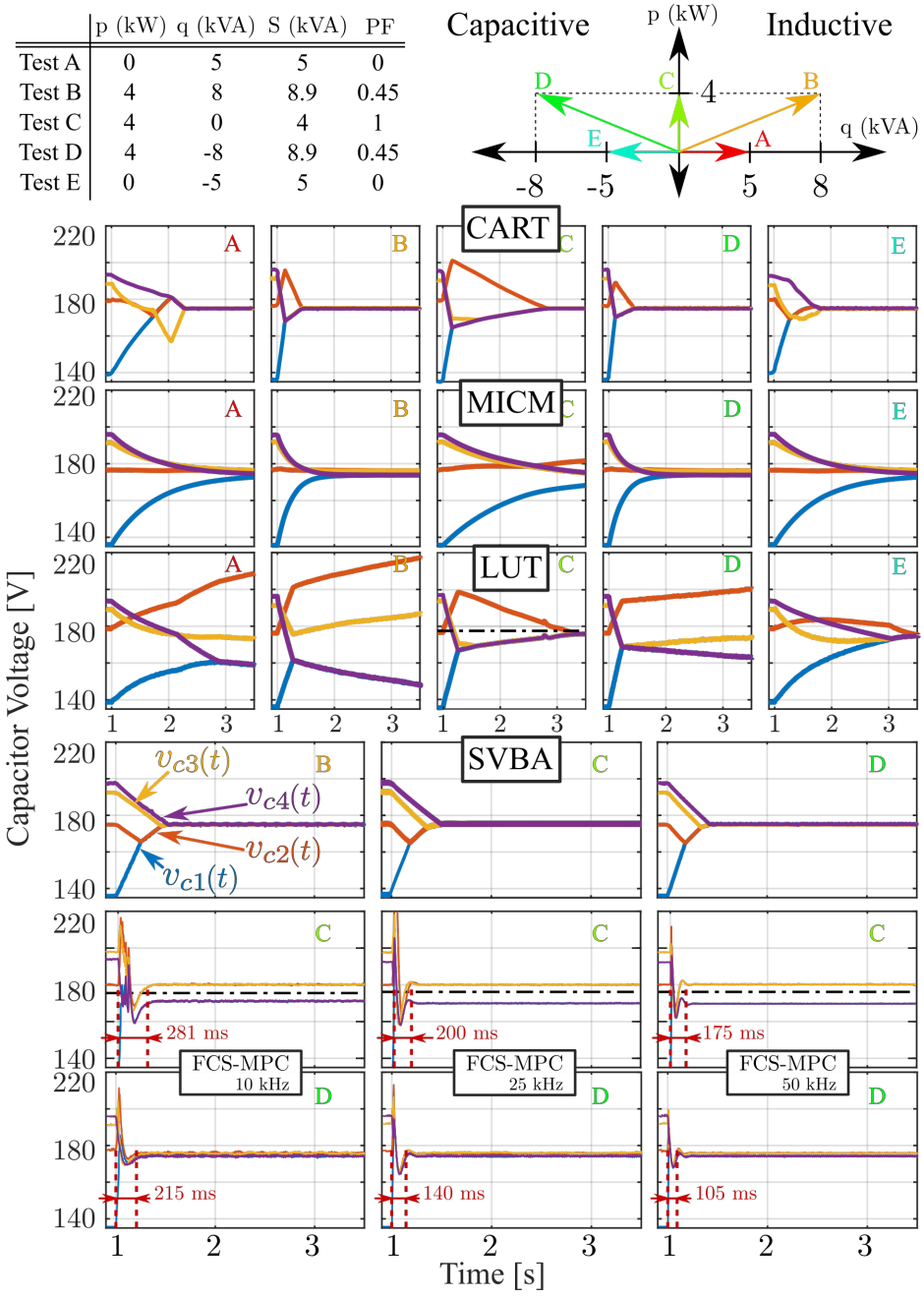

Figure 2.54 Capacitor voltages evolution starting from an unbalanced situation $v_{d1} = -40, v_{d2} = 60, v_{d3} = -5$ for all the considered approaches under different tests whose power references are shown at the top of the figure. $v_{dc} = 700$ V.

Table 2.17 THD values of the currents (Fig. 2.52) and number of commutations over a grid period (Fig. 2.53).

Approach		THD (%)	Nº Commt
CART		4.6	550
LUT [117]		4.6	645
SVBA [134]		7.01	935
FCS-MPC [89]	10 kHz	13.42	210
	25 kHz	5.10	540
	50 kHz	2.54	1100
OICM [116]		5.40	1600
MICM [116]		4.2	1333

under different active and reactive power references—and thus different power factor values—, as it is shown at the top of Fig. 2.54. Note that these test results are exhibited only for the capacitor voltage balance as it is the feature where the considered modulations exhibit most differences. This figure exhibits the main advantage of the CART-based approach in comparison with the previously considered LUT–based one, that is the wider range of operating points. In order to extend the validity of the LUT approach, the test cases should cover the full operating range and the number of tables would increase. In this comparison, power factor equal to unity was the only test considered in the look-up table generation (Test C), and therefore the balancing is not guaranteed for different conditions, as it happens with tests A,B and D. On the contrary, due to the extended training data set, the qualitative information used for input-output data and its generalization capability, the CART approach is capable of achieving voltage balance capabilities under these scenarios, achieving a more flexible implementation of the optimization problem originally computed. It is worth mentioning that the power factors of tests B and D were not considered explicitly in the training dataset. Therefore, the CART method has properly generalized the results in such a way that it fulfills the control objectives under these conditions. Regarding the remaining approaches, FCS-MPC exhibits the fastest balancing no matter the sampling frequency or the test considered—that is why only two tests for the three sampling frequencies have been considered—, however a steady-state error appears in the capacitor voltages. Alternatively, SVBA shows improved balancing capabilities than the CART approach but it comes at the cost of increased current distortion and number of commutations (see Table 2.17). For the sake of clarity, only MICM approach is depicted as its balancing capabilities are better than the OICM. It is shown that MICM has the slowest balancing of the considered approaches without reaching zero-steady state error.

In summary, the proposed method achieves an acceptable balancing settling time without compromising other performance indicators, while reaching a wide set of operating points. Consequently, these simulations prove the good and pseudo-optimal behaviour of the proposed approach.

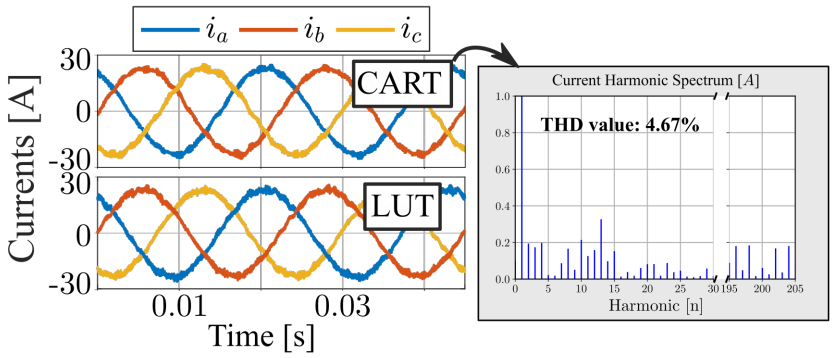

Figure 2.55 Three-phase currents in steady-state for the considered approach (left-top) and the LUT-based approach (left-bottom). Distribution of the harmonics amplitude for phase a of the proposed approach and resulting THD value (right). LUT–based approach yielded similar harmonic spectrum and a THD value of 4.61%. $v_{dc}^{*} = 800\,V$, $R = 60\,\Omega$, $q^{*} = 0\,kVA$.

Experimental results

To further prove the feasibility of the current approach, some experimental results are presented using the same system than the previous sections (Fig. 2.21). The system parameters are the same than the ones exhibited in Table 2.15, and the trees are the same than those obtained for the simulations.

Given that the LUT comparison with the other techniques has already been exhibited in the previous section, this section is focused on validating the performance of the approach in comparison with the LUT-based one in a real converter.

The first results are shown in Fig. 2.55, where the three-phase currents in steady-state conditions ($v_{dc}^{*} = 800$V, $R = 60\,\Omega$ and $q^{*} = 0\,k$VA) are depicted for the CART approach and the LUT-based one. It is worth mentioning that the LUT-based approach uses the same tables generated for the simulation, which are the same ones than those used in the previous section (Sect. 2.3.6). Consequently, the cost function of the LUT-based approach (2.136) is not the same than the one used for the CART-based one (2.141), although Fig. 2.55 depicts that no noticeable difference appears in steady-state due to this. The total harmonic distortion (THD) value of the current is shown for the CART-based approach, but the LUT-based one presents a similar result (THD$= 4.61\%$). For these conditions, and similarly to the obtained results in simulation (Table 2.17), the CART-based proposal reduces slightly the number of commutations compared to the LUT-based one (CART: 580 vs LUT: 620). Again, this could derive from the generalization capability of CART that unifies the same criterion when a particular set of inputs is given, in contrast to the LUT.

In order to exhibit the flexibility of the proposal based on CART, three tests are performed. The first test, called Test 1, modifies the dc-link voltage reference (v_{dc}^{*}) and the dc load resistor (R) in order to modify the active reference power (p^{*}). This test was in fact already carried out for the LUT-based approach, which fulfilled the control objectives. Therefore, this test is carried out to show that this proposal has a similar performance than the LUT-based one when the considered conditions are the same than those for which the

Table 2.18 Load and dc-link voltage values used in Test1.

$t: 0 \rightarrow 1.5$		$t: 1.5 \rightarrow 2.2$	$t: 2.2 \rightarrow 2.9$	$t: 2.9 \rightarrow 4.4$		$t: 4.4 \rightarrow 5.5$
v_{dc}^* (V)	$R\ (\Omega)$	$R\ (\Omega)$	v_{dc}^* (V)	v_{dc}^* (V)	$R\ (\Omega)$	$R\ (\Omega)$
700	120	60	$700 \rightarrow 800$	800	60	120

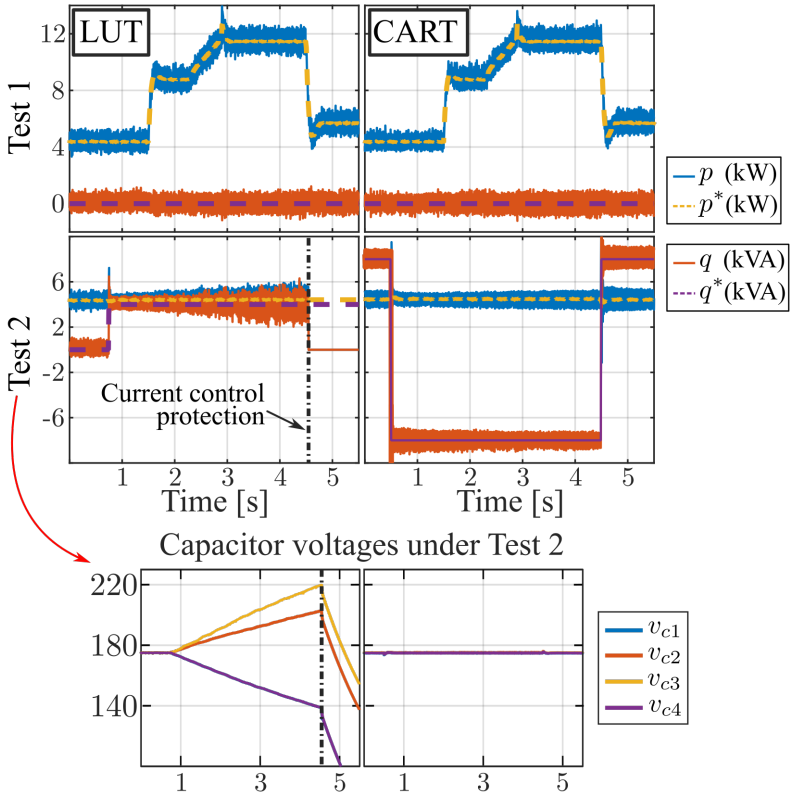

Figure 2.56 Active and reactive power behaviour for LUT-based and CART-based approach under two different tests. The capacitors voltage evolution during Test2 are also depicted.

LUTs were obtained. The modified parameters and the time they take place are shown in Table 2.18. This test is depicted in Fig. 2.56 (top) where it can be seen that the changes that takes place in the active power reference are properly tracked by the inner controller.

The second test, called Test 2 and also depicted in Fig. 2.56, considers a change in the reactive power while keeping the active power constant. The intent of such a test is to evaluate the algorithm when a power factor value different from unity is given. The LUT-based approach is evaluated under a jump from 0 to 4 kVAr at $t = 0.7$ s and, given that the LUT has not been obtained for these conditions, the capacitor voltage regulation is not achieved, as it can be seen at the bottom of Fig. 2.56. The experiment is halted at

$t = 4.5$ due to the large current distortion generated by the high capacitor voltage unbalance. In contrast, a jump from 7 kVAr to -7kVAr is given at $t = 0.5$ s, and back to 7 kVAr at $t = 4.5$ s for the CART-based approach with no effect on the capacitor voltage regulation. In comparison with the LUT-based approach, during Test 2, no increase on the power ripple nor effect on the capacitor voltage regulation are seen.

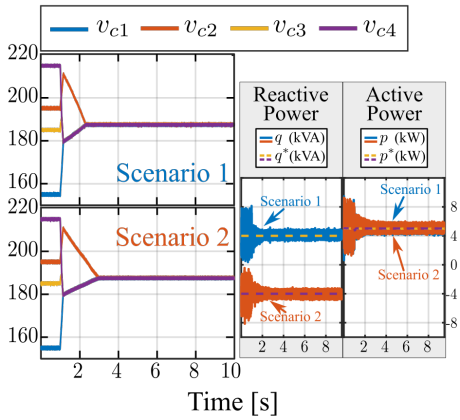

Figure 2.57 Capacitor voltage evolution from unbalanced situation for CART approach.

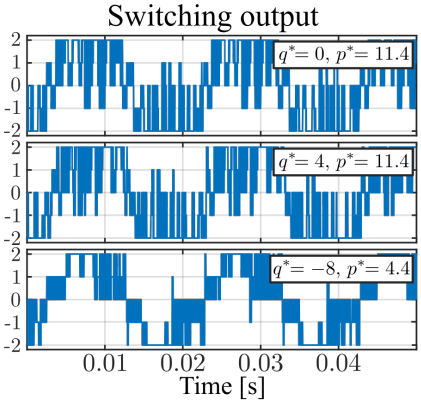

Figure 2.58 Switching output for phase a under steady-state conditions for different values of active and reactive power.

The third test is shown in Fig. 2.57 and performed in order to further depict the extended range of operation of the CART-based approach. For this, two scenarios are considered under operating conditions that where not covered by the CART training dataset (power factor equals to $1/\sqrt{2}$, capacitive and inductive). Besides, it is considered that the capacitor voltage values start from an unbalanced condition and, at $t = 1$ s, the balancing is activated. It can be clearly seen that the capacitor voltages are regulated towards zero in short time and remain there while fulfilling the power tracking objectives. Note that the initial large ripple that appears in the power tracking is due to the initially forced capacitor voltage unbalance.

Lastly, the switching output for one phase in steady-state for three different operating points is shown in Fig. 2.58, where the different levels used for the modulation can be noticed

Conclusions and future lines of research

This proposal exhibits a method to implement the modulation stage for 5-level DCCs. The method is based on a linear, mixed-integer optimization problem that is solved offline and its solutions are used to train classification and regression trees (CARTs) that are later used during online operation. In this way, an implementation with low-computationally burden of an optimal modulation approach is achieved. Furthermore, the resultant controller can cover a wide range of operating conditions due to three facts: 1) the generalization capabilities of CARTs; 2) the input-output data have been chosen in order to capture

qualitative information about the state of the system; and 3) the training set is not limited to an operating point but to a range of them. The simulation section exhibits improvements in several performance indicators when compared with other solutions, whereas the experiments were carried out under several operating conditions, including some that were not covered in the training sets. As a result, the carried out tests exhibit the feasibility of this approach to reach wider range of operating point conditions while keeping a satisfactory behaviour with simple implementation.

Future lines of research could cover the inclusion of other performance indicators into the cost function in order to obtain an improved algorithm, such as the presence of low-order harmonics in the current or common-component in the output voltage. Additionally, the steps carried out in the derivation of this optimal modulation can be easily extended to other multilevel converter topologies as the optimal criteria considered here can be applied in general terms.

3 Contributions to Cascaded and Modular Converters

When you want to know how things really work, study them when they're coming apart.

William Gibson

The previous chapter exhibited the contributions in DCCs, which were classified in the introduction section as a kind of converters that had one single dc-link. This chapter will expose the contributions done in the field of cascaded and modular converters, which, in contrast to DCC, have multiple dc-links, which allow them to present a modular configuration. This topology of converters has shown high potential in integrating medium to high voltage energy sources to the grid, alleviating the challenges associated with the conventional converters [138]. Distinctive features, such as modularity, redundancy and scalability, among others, arise when compared with conventional converters.

Nowadays, they have been the scope of many researchs for HVDC applications as their modularity and scalibility allow them to be stacked in such a way that large voltage magnitudes can be reached [139–142]. There are some differences in terms of implementation and functionality between the cascaded and modular converter. However, this chapter analyzes both as the general idea and operation principle is similar between them. In fact, there are some papers that presents hybrid configurations of cascaded converters with modular converters [143–145].

3.1 Principle of operation

Cascaded and modular converters share a similar concept in terms of layout, that is, the use of serialized modules that comprise a branch, and, at least, one inductor for each phase. This configuration with a proper control scheme allows each branch to be regarded as a controllable current source [146]. In three-phase grid-connected cascaded converters,

each branch corresponds to a phase, where each module has its own dc-link, and thus the voltage branch is capable of reassembling the grid voltage and current. Alternatively, three-phase grid-connected modular converters have two branches per phase—an upper and a lower branch—whose middle point is connected to the grid, and their upper and lower points are connected to a DC bus that provides energy to power up the three phases. A single-phase scheme of these two topologies of converters is shown in Fig. 3.1. With the modular configuration, the switching has to be performed in such a way that the added voltage of the two arms interacts with the DC bus voltage, whereas the difference defines the voltage at the point connected to the grid. The circulating current (i_{circ}) is a phenomena that takes place in modular converters due to the former, and it corresponds to the current that circulates equally through the two branches and the DC bus. This current has a DC component that transports the energy from the DC bus to the modules [147].

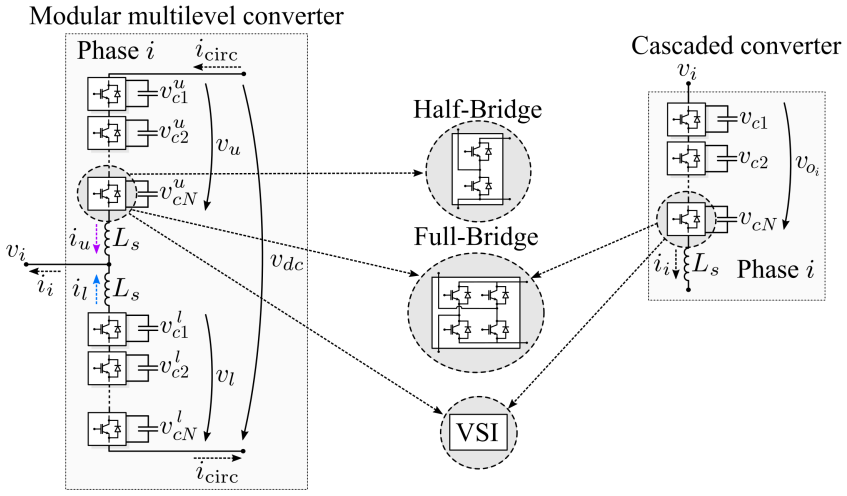

Figure 3.1 Scheme of a single-phase cascaded and modular converter. Parallel connection of these circuits builds up a three-phase converter.

One could point out that, in order to set a three-phase system, modular converters require six branches, whereas the cascaded converter only requires three. This is true, but the cascaded converter branches have to be capable of generating positive and negative voltages in order to modulate sinusoidal grid voltages. This means that, at least, H-bridge modules, which have four switches and two control signals, have to be used. On the contrary, modular converters can use half-bridge modules, which use only two switches and one control signal [148]. As shown in Fig. 3.1, a voltage source inverter (VSI) could be used as a module for both topologies [149, 150]. Noting v_{cn} as the dc-link voltage of the module, H-bridge modules—also referred as full-bridge—have four switching positions (2^2) but three possible output voltages $v_{on}^{\text{FB}} = -v_{cn}, 0, v_{cn}$, while half-bridge ones have only two switching positions and two possible output voltages $v_{on}^{\text{HB}} = 0, v_{cn}$. Besides, a branch composed of two full-bridges with equal dc-link voltage will present five possible output voltages, but sixteen switching positions. The inherent redundancy in a full-bridge

module has been used in the literature to provide active thermal management [151](see Sect. 2.3.5), whereas the redundancy that appears when two or more modules are serialized with equal capacitor voltage is usually used for balancing purposes as it is exposed later [152], similarly to the redundant switching vectors of the DCC.

In the following, the full-bridge module will be used for the cascaded converter, which is denoted as cascaded H-bridge (CHB) converter. Similarly, the half-bridge module will be used for the modular converter, which will be referred as modular multilevel converter (MMC). According to this, a CHB converter with N H-bridges per phase can output $2N-1$ levels, whereas a MMC with N modules—called submodules (SM) from now on—can output N levels.

3.1.1 Switching states

The number of switching states, for cascaded and modular converters, depends on the type of the module and the amount of them. As it have been said, FB modules can generate three possible outputs, whereas HB ones have only two.

A three-phase CHB converter presents a similar space vector region than the one exhibited for DCC (Fig. 2.4), where the redundant switching vectors due to same phase-phase generation can be included [153]. However, when more than one module is serialized in a phase, additional redundancies can result for that phase. For example, two serialized modules with equal capacitor voltage can achieve the same v_{o_i} by connecting one module and bypassing the other, or the other way around. This feature is used to achieve capacitor voltage balancing as it will be exposed later. Besides, there are additional degrees of freedom as every HB module has two switching positions that output 0 V. The only difference between them is in the used switching devices. Either by connecting the two upper devices or the two lower ones, the module is bypassed, although the current would go through different switching devices. This feature is used in the literature to balance the switching device usage, providing the already mentioned thermal management [151]. Consequently, in CHB converters, the space vector region can be determined by the possible voltage outputs each phase can generate. The switching state generation is later performed for each phase considering the available switching options and capacitor voltage balance purposes [154].

In the case of N-level MMC, a similar procedure is carried out. However, due to its modularity, it is expected that large amount of SM are seen in this topology (some HVDC applications count for more than 400 SMs [155]). For this, it is not common to use SVM in MMC as an unfeasible space vector region can derive from it. Nevertheless, some works have focused on simplifying the SVM implementation for MMC [156, 157], by dividing the regions into smaller ones that are computationally affordable, among other possible solutions. The existence of two arms in MMCs makes the switching state determination different from the cascaded converter, that is, two voltage commands are given: one for the upper arm (v_u^*) and another for the lower one (v_l^*). Note that, considering the scheme shown in Fig. 3.1, the modulated voltage has to hold the following equation

$$v_u + v_l + L_s \frac{d(i_u - i_l)}{dt} = v_{dc} \tag{3.1}$$

where the circulating and output currents are defined as $i_{\text{circ}} = i_u - i_l$ and $i_i = i_u + i_l$, respectively. Additionally, if the output voltage v_i is measured with respect to an imaginary middle dc-link point, two Kirchhoff's equations can be obtained that determine how the output voltage is commanded

$$\left.\begin{array}{ll} v_i & = -L_d \frac{di_u}{dt} - v_u + \frac{v_{dc}}{2} \\ v_i & = -L_d \frac{di_l}{dt} + v_l - \frac{v_{dc}}{2} \end{array}\right\} \; v_i = L_d \frac{di_i}{dt} + v_l - v_u \,, \tag{3.2}$$

which means that imposing a difference between the modulated voltages of each arm (v_u and v_l), the output voltage (v_o) is commanded. Therefore, the controllers would define a voltage command for the upper v_u^* and lower v_l^* arms taking into account (3.1)–(3.2) to regulate the output current and the circulating current simultaneously.

Once these voltage commands are determined, and given that there are only two possibilities for each SM, the modulation takes place separately for each arm. The latter usually involves which SMs are selected to be bypassed or connected according to their capacitor voltage value and the sign of the arm current (i_u or i_l) as it will be explained later. In line with this, the stacked capacitor voltage value of the connected SMs must reassemble the corresponding arm voltage command.

In order to simplify this process and avoid large computations with large values of N, a normalization procedure is carried out. With this, the voltage command no longer expresses the desired voltage to modulate but the number of SMs to be connected

$$v_{u_z}^* = \frac{v_u^*}{\bar{v}_c} \,, \quad v_{u_z}^* \in [0,N] \tag{3.3}$$

$$v_{l_z}^* = \frac{v_l^*}{\bar{v}_c} \,, \quad v_{l_z}^* \in [0,N] \,, \tag{3.4}$$

where $v_{k_z}^*$ for $k = u,l$ refers to the normalized voltage command for arm k, and $\bar{v}_c$ refers to the average capacitor voltage. Regarding the latter, there are two usual values that the literature considers:

$$-\text{Average capacitor voltage of phase } i \rightarrow \bar{v}_c = \frac{1}{2N} \sum_{k=u,l} \sum_{n=1}^{N} v_{cn}^k \tag{3.5}$$

$$-\text{Average capacitor voltage of arm } k \rightarrow \bar{v}_c^k = \frac{1}{N} \sum_{n=1}^{N} v_{cn}^k \,, \tag{3.6}$$

where the first one is known as direct modulation and the second one as indirect modulation. The first one assumes that all SM capacitor voltages within the same phase can be approximated to be equal, while the second one does it for each arm. In spite of the hard of the assumption, it is expected that the capacitor voltage variations between them is compensated in average thanks to the large number of SMs used, and the computations are considerably simplified [147]. Nevertheless, one technique has been developed in this work [158] that tries to compensate for the inherent modulation error that this normalization step causes. This contribution will be explained later in this chapter.

Fig. 3.2 shows examples of redundancy within the same phase i for a five-level CHB converter, and within the upper arm for a MMC with three SMs. Both cases assume that the capacitor voltages are equal with value v_{dc}, and that it is desired to impose an output voltage of v_{dc}. Note that, for the MMC, there are three possible switching states, whereas the CHB converter has two possible positions. Similarly to the switching vectors in the SVM region, the larger the voltage to be modulated, the lower the number of redundant switching positions that achieve such value. For example, in Fig. 3.2 for the MMC, making $v_u = 3v_{dc}$ is only possible with one position, whereas for the CHB converter, making $v_{o_i} = 2v_{dc}$ can only be achieved by connecting both CHBs.

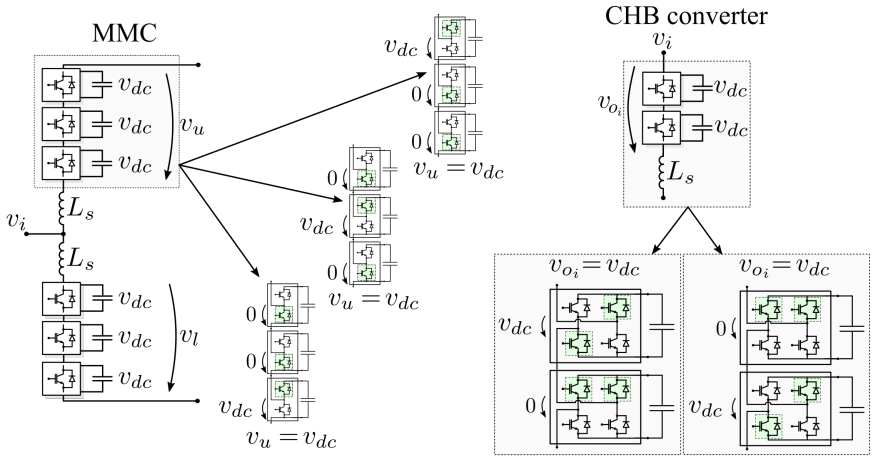

Figure 3.2 Examples of redundancy within the upper arm for a MMC with three SMs when $v_u = v_{dc}$ (left), and within one phase for a five-level CHB converter when $v_{o_i} = v_{dc}$ (right).

At this point, any of the well-known modulation approaches used for multilevel converters can be applied, either to CHB converters or MMC, considering the normalized voltage commands expressed in (3.3)–(3.4) [159]. However, in MMC, it is worth noting that the most common CB-PWM approaches—LS-PWM and PS-PWM—require a carrier for each SM [160]. Hence, in an attempt to reduce the implementation burden of the control of MMC with large number of SMs, a modulation approach is commonly considered due to its simplicity and feasible results. This approach is usually referred as nearest level control (NLC) or nearest level modulation (NLM) as it takes the rounded values of the normalized voltage commands (3.3)–(3.4), and uses them as the number of SMs to connect for each arm during the whole switching period. As a result, no carriers are required and the implementation is only concerned about selecting the preferable SMs to be connected. It is worth noting that some modulation error appears due to this rounding effect. However, for large enough values of N, this effect is almost negligible.

3.1.2 Output current control

Regarding the phase current (i_i in Fig. 3.1) regulation, any of the already mentioned current controllers can be used to achieve such purpose (see Sect. 1.2.4). For this, note that the CHB converter current dynamics is equal to that of a standard VSC, that is

$$v_i = v_{o_i} + L_s \frac{di_i}{dt} + v_{nN} \quad \text{for } i = a,b,c\,, \tag{3.7}$$

where v_i is the phase voltage (measured with regards to the neutral point N of the grid), and v_{nN} is the voltage between the neutral of the CHB converter and the neutral of the grid. Hence, the output voltage v_{o_i} can be used to regulate the phase current i_i.

In the case of MMC, Eq. (3.2) expresses similar dynamics, where the difference between the lower voltage (v_l) and the upper voltage (v_u) determines the control action. Defining the control signals for each phase i as

$$v_u^i \coloneqq -\frac{v_{\text{dif}}^i}{2} + \frac{v_{\text{com}}^i}{2} + \frac{v_{dc}}{2} \tag{3.8}$$

$$v_l^i \coloneqq \frac{v_{\text{dif}}^i}{2} + \frac{v_{\text{com}}^i}{2} + \frac{v_{dc}}{2}\,, \tag{3.9}$$

v_{dif}^i would represent the voltage command given to regulate the output current i_i, whereas v_{com}^i is used to regulate the circulating current (see Eq. 3.1), as it will be exposed later.

3.1.3 Capacitor voltage balancing

This section exhibits how the capacitor voltage balance task can be tackled for either CHB and MMC converters. Given the particular modularity of both topologies, the capacitor voltage balance can be seen as a task of power sharing between modules. At steady state, and assuming same DC-side conditions for all modules, the average power that is delivered/absorbed by each module has to match that of its load, otherwise the capacitor voltage value would not remain constant, and unbalances would appear.

In both topologies, the existence of several modules in each phase creates additional control objectives in terms of capacitor balance. In the case of single dc-link systems, such as the DCC previously covered, the designed controllers had to balance the capacitors considering the interaction of each phase with the dc-link. In contrast, in CHB converters and MMC, there exist two types of unbalances that can be classified as follows

- **Capacitor voltage unbalance between different phases**. The control objective is to regulate the average capacitor voltage value of all modules in each phase to be equal among the three phases. This objective can be synthesized using two variables as it will be exposed later.
- **Capacitor voltage unbalances between modules within the same phase**. For CHB converters, these unbalances can be modelled as the difference between the capacitor voltage of each module and the average of the same phase. However, for MMC, these unbalances are usually separated in two, the unbalances among SMs within the same arm, and the unbalance between both arms. Again, the former are

modelled from the differences between the arm average capacitor voltage and the individual ones, whereas the latter is modelled from the difference between the average value of each arm.

In-phase capacitor voltage balance

The balancing of modules within the same phase for CHB converters, or within the same arm for MMC can be treated similarly. In this regard, the redundancy mentioned before and exampled in Fig. 3.2 is used to achieve this task. In general terms, once the normalized voltage command is known—for one arm in MMC or one phase in CHB converters—all possible switching configurations that fulfill such value are considered and the most beneficial one is selected. This process must consider the sign of the current that goes through the modules, as it will dictate if the connected modules are being charged (input current to the module dc-link) or being discharged (output current from the module dc-link). To carry out this process, it is common to use a sorting algorithm the sorts the modules according to their capacitor voltage value [161, 162].

For example, considering the CHB converter case depicted in Fig. 3.2, if the current is positive—it inputs the converter—the connected module would be charged. Therefore, the module with the smallest capacitor voltage should be prioritized to be connected. In the opposite case, were the current to be negative—it outputs the converter—the connected module would be discharged, and thus the one with the largest capacitor voltage should be prioritized.

Note that CHB converters for low modulation indexes—that is, relatively low values of $\frac{v_{o_i}}{v_{dc}}$—can decide whether to bypass serialized modules, or to modulate a positive voltage with one module and compensate it with the negative voltage of another. In the second case, it is possible to accelerate the balancing task or to achieve more steady capacitor voltage waveforms. In any case, the considered modulation approach should take this feature into account [163–165].

Alternatively, it has been shown that PS-PWM can achieve power sharing, equalization of losses and improved harmonic performance without the requirement of a sorting algorithm [138].

For MMC, the sorting algorithm is a keystone for the balancing between SMs within the same arm. This feature along with the circulating current control are the ones in charge of regulating the capacitor voltage values of the SMs within one phase [166, 167]. In the following, one approach for capacitor voltage balance extracted from [168] is exhibited.

Focusing on a single phase, let us denote the capacitor voltage of SM_n in arm k as v_{cn}^k for $n = 1,\ldots,N$ and $k = u,l$. Similarly, the average capacitor voltage of all SMs within arm k is referred as $\bar{v}_c^k$, whereas the SM average for all SMs in the phase is referred as $\bar{v}_c$

$$\bar{v}_c^k = \frac{1}{N}\sum_{n=1}^{N} v_{cn}^k \quad \text{for } k = u,l \tag{3.10}$$

$$\bar{v}_c = \frac{1}{2N}\sum_{k=u,l}\sum_{n=1}^{N} v_{cn}^k \,. \tag{3.11}$$

In the one hand, the sorting algorithm selects the SMs whose v_{cn}^k is more diverged from the average—the ones with the lowest values if the arm current charges the SMs, or the ones with the highest values otherwise. On the other hand, the arm voltage command v_k^* is modified according to the difference between $\bar{v}_c^k$ and the desired capacitor voltage (v_c^*)—usually set to $\frac{v_{dc}}{N}$. In this way, a term—referred as Δv_k^*—proportional to this difference and the sign of the arm current is added to the voltage command of that arm. The latter introduces one loop for each arm with the following expressions

$$\Delta v_u^* = \text{sign}(i_u) K_p^u \left(v_c^* - \bar{v}_c^u\right) \tag{3.12}$$

$$\Delta v_l^* = \text{sign}(i_l) K_p^l \left(v_c^* - \bar{v}_c^l\right). \tag{3.13}$$

This control scheme is depicted in Fig. 3.3, where it can be seen the control scheme to regulate both $\bar{v}_c^k$ towards v_c^*, and the sorting algorithm that regulates the SMs voltage within one arm to be equal.

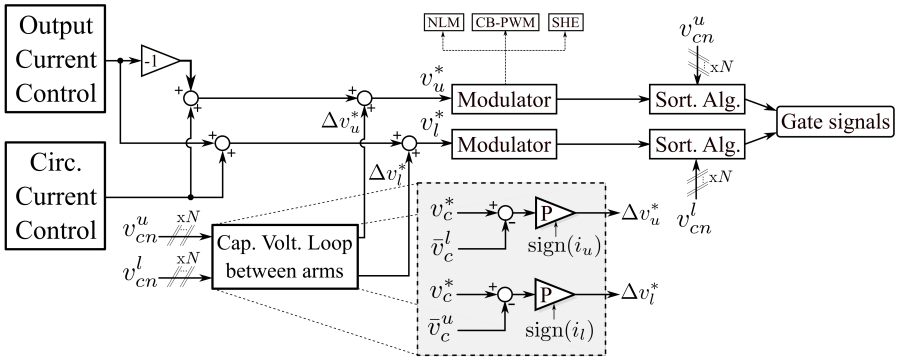

Figure 3.3 Control scheme of a single-phase MMC with details of the control loop to balance capacitors between arms. Extracted from [168].

Inter-phase capacitor voltage balance

These unbalances appear in systems with more than one phase, and it is the result of an improper power sharing/consumption between phases. For the remaining of this section, the previous variables are referred for each phase $i = a,b,c$ with the super-index $\square^i$.

For CHB converters, this unbalance takes place when power consuming/generating units are attached to the dc-link of each module, and the total power consumed/generated for each phase does not match between them. In fact, the in-phase balance may also suffer from load/source inequalities, which can be compensated with a proper balancing approach, as mentioned before, but within some boundaries of unmatched power [169]. One well-known approach to compensate the inter-phase unbalance is by means of using zero sequence injection [170, 171], which consists in adding a common component—that will be referred as x—to the three voltage commands v_{o_i} simultaneously. Note that this is equivalent of using the redundant switching vectors, that were explained in Sect. 2.1.2,

for DCC. In CHB converters, for example, a positive zero-sequence injection means an increase of the voltage command, which involves either more modules connecting their dc-link positively, or less modules connecting their dc-link negatively. Following this example, a positive zero-sequence injection added when a phase current is also positive would mean an increase of the power injected to the corresponding phase. Given that the addition of the three phase currents has to be zero, the power that is injected/subtracted in one phase due to the zero-sequence is subtracted/injected from/to the others. This can be mathematically expressed as

$$\left.\begin{aligned} p_a + \Delta p_a &= (v_{o_a} + x) i_a \\ p_b + \Delta p_b &= (v_{o_b} + x) i_b \\ p_c + \Delta p_c &= (v_{o_c} + x) i_c \end{aligned}\right\} \rightarrow \Delta p_a + \Delta p_b + \Delta p_c = x(i_a + i_b + i_c) = 0 \qquad (3.14)$$

where p_i and Δp_i for phases $i = a,b,c$ are the active power and its increment of it due to the zero-sequence voltage injection, respectively. A contribution in this regard has been made [172], where a rule for the zero-sequence voltage determination for CHB converters is proposed along with a conservative derivation of the boundaries for power mismatch, inside which the proposal is capable to achieve inter-phase balance. This contribution is exposed later in this chapter.

In the case of MMC, it is the circulating current the factor that introduces power in each phase, as the three phases are all connected to the same DC bus. Hence, the inter-phase unbalance is the result of an improper circulating current regulation. Indeed, the circulating current must have a DC component to power-up the SMs within each phase [173]. In this regard, some works have focused on eliminating the AC component of this current as it introduces additional losses [174].

Considering the above, the inter-phase unbalance in MMC is an issue of delivering the proper power to each phase by means of the circulating current. This issue also takes place in single-phase systems where the SMs need a specific amount of power to work properly. Note that, at steady-state conditions, the power delivered from the DC bus corresponds to the one delivered to the AC side. Given that the DC bus is common for the three phases and they are connected in parallel, the circulating current regulation of one phase has no effect on the others. Therefore, the inter-phase unbalance can be regarded as a matter of regulating three independent circulating currents in such a way that variable $\bar{v}_c$ for each phase—referred as $\bar{v}_c^i$—goes towards the reference v_c^* [175].

By means of the DC component of the circulating current, the average capacitor voltage of the SMs within one phase ($\bar{v}_c^i$) can be regulated. Therefore, a cascaded controller can be formulated as it follows [168]. Focusing on a single-phase scheme, the dynamics of the circulating current are expressed in (3.1) and summarized as

$$L_s \frac{di_{\text{circ}}}{dt} = v_{dc} - v_u - v_l \,, \qquad (3.15)$$

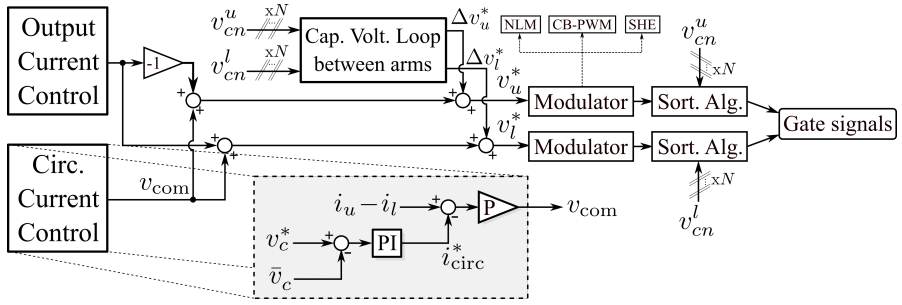

Figure 3.4 Control scheme of a single-phase MMC with details of the control loop to balance the average capacitor value in one phase. Extracted from [168].

which is obtained by considering the voltage drop along the phase. Recalling the signal control definition from (3.8)–(3.9), the i_{circ} dynamics are expressed as

$$L_s \frac{di_{\text{circ}}}{dt} = -v_{\text{com}} \,, \tag{3.16}$$

where a simple proportional loop can regulate i_{circ}. Indeed, by defining the following control law with K_p^{circ} as proportional gain

$$v_{\text{com}} = K_p^{\text{circ}}(i_{\text{circ}} - i^*_{\text{circ}}) \,, \tag{3.17}$$

the circulating current tracks its reference i^*_{circ}. The remaining part is to determine the circulating current reference, which can be done considering the $\bar{v}_c$ regulation, that is, using a PI controller with control parameters K_p^{bal} and K_i^{bal}. In this way,

$$i^*_{\text{circ}} = K_p^{\text{bal}}(v^*_c - \bar{v}_c) + K_i^{\text{bal}} \int_0^t (v^*_c - \bar{v}_c) d\tau \,. \tag{3.18}$$

It is worth mentioning that, as similarly exposed in the cascaded configuration section (Sect. 1.2.4), the outer controller, i.e. the regulation of $\bar{v}_c$, has to be tuned in such a way that its control bandwidth is much smaller than the inner one, i.e. the bandwidth of the regulation of i_{circ}. Fig. 3.4 depicts this control scheme along the controllers exposed in Fig. 3.3 for a single phase.

3.2 Modulation algorithm for inter-phase balancing in CHB converters

This proposal is a contribution of this dissertation that was published in [172], and it presents an algorithm to compute the zero-sequence injection in three-phase CHB converters to tackle with the balancing between phases. For this approach, each module of the converter has a dc-link load, whose total phase power consumption is not matched among phases, resulting in an inter-phase unbalance. The proposal solves this unbalance, achieving proper power sharing between phases. A further analysis is carried out that

results in conservative power boundaries, inside which the approach is mathematically proved to be capable of achieve balancing. Besides, a modification is further introduced that improves the converter efficiency as it will be shown by simulation results.

3.2.1 System model and proposed control law

The proposal presented in this section is modelled and discussed for a five-level CHB converter, but it can be extended to any number of levels of the same topology. The system is composed of two modules per phase, and it is connected to the grid through an L filter. The power consumption given in each module are modelled as a current source that drains current from the capacitor, whose capacitance is equal to C for all modules. The voltage that it is modulated in each phase is referred as v_{o_i} for $i = a,b,c$, the grid voltages are referred as v_i, and the phase currents are denoted as i_i. Additionally, the capacitor voltage and current consumption of each cell are expressed as v^i_{cn} and I^i_{cn} for $i = a,b,c$ and $n = 1,2$, respectively. Note that index n refers to the number of the module, that is $n = 1$ for the upper module and $n = 2$ for the lower one. This scheme is depicted in Fig. 3.5.

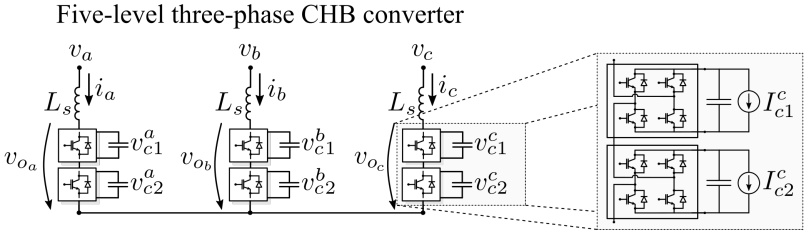

Figure 3.5 Scheme of a five-level CHB converter.

Following this nomenclature, the capacitor voltage dynamics for any module n in any phase i can be expressed as follows

$$C\frac{dv^i_{cn}}{dt} = i_i v_{o_{in_z}} - I^i_{cn} \quad \text{for } n = 1,2 \tag{3.19}$$

where $v_{o_{in_z}} = -1,0,1$ refers to the normalized output voltage of the module depending on the switching position. In this regard, the output of the phase is equal to the addition of the output voltages of the two modules, that is, $v_{o_{i_z}} = v_{o_{i1_z}} + v_{o_{i2_z}}$.

To model the phase unbalance, the average capacitor voltage of each phase—denoted as $\bar{v}^i_c$—is considered along with the total current that is extracted from both dc-links—denoted as I^i_c. In this way,

$$\bar{v}^i_c = \frac{v^i_{c1} + v^i_{c2}}{2} \tag{3.20}$$

$$I^i_c = I^i_{c1} + I^i_{c2}\,. \tag{3.21}$$

With this, the dynamics of $\bar{v}_c^i$ can be derived by replacing (3.19) into the derivative of (3.20)

$$C\frac{d\bar{v}_c^i}{dt} = \frac{1}{2}(v_{o_{iz}} i_i - I_c^i)\,. \tag{3.22}$$

Additionally, the phase unbalance, i.e. the unbalance between the three phases, can be characterized using two error signals, which are defined as follows

$$v_{d1} \coloneqq v_{dc} - \bar{v}_c^a \tag{3.23}$$
$$v_{d2} \coloneqq v_{dc} - \bar{v}_c^b\,, \tag{3.24}$$

where $v_{dc} = 1/3\sum_{i=a,b,c}\bar{v}_c^i$. Considering the derivative of these error signals, and using (3.22), the following expressions are obtained

$$C\frac{dv_{d1}}{dt} = \frac{1}{6}(-2i_a v_{o_{a_z}} + i_b v_{o_{b_z}} + i_c v_{o_{c_z}} + \gamma_1) \tag{3.25}$$
$$C\frac{dv_{d2}}{dt} = \frac{1}{6}(i_a v_{o_{a_z}} - 2i_b v_{o_{b_z}} + i_c v_{o_{c_z}} + \gamma_2) \tag{3.26}$$
$$\gamma_1 = 2I_c^a - I_c^b - I_c^c$$
$$\gamma_2 = -I_c^a + 2I_c^b - I_c^c,$$

where γ_n expresses the unmatched currents consumption, that is, it would be equal to zero if the currents consumption were matched between phases. Lastly, the addition of a zero-sequence component can be modelled by considering that a term x is added to the three output voltages $v_{o_{iz}}$ simultaneously. Replacing $v_{o_{iz}}$ for its corresponding value with the zero component added, i.e. $v_{o_{iz}} + x$, the following dynamic of the error signals are obtained

$$\frac{dv_{d1}}{dt} = \frac{1}{6C}(-2i_a v_{o_{a_z}} + i_b v_{o_{b_z}} + i_c v_{o_{c_z}} + \gamma_1 - 3i_a x) \tag{3.27}$$
$$\frac{dv_{d2}}{dt} = \frac{1}{6C}(i_a v_{o_{a_z}} - 2i_b v_{o_{b_z}} + i_c v_{o_{c_z}} + \gamma_2 - 3i_b x)\,, \tag{3.28}$$

which expresses how the added zero-sequence component can affect the error signals. To derive how to compute the value of x, a Lyapunov function candidate is proposed as

$$V = |v_{d1}| + |v_{d2}|\,, \tag{3.29}$$

whose derivative has to be negative in order to make these signals go to zero. Note that (3.29) is not differentiable when either $v_{d1} = 0$ or $v_{d2} = 0$. However, given that a formal proof of stability is not pursued, function (3.29) will be used as inspiration for a new control strategy. Assuming constant sign of v_{d1} and v_{d2} around the period of derivation,

$$\frac{dV}{dt} = \text{sign}(v_{d1})\frac{dv_{d1}}{dt} + \text{sign}(v_{d2})\frac{dv_{d2}}{dt}\,. \tag{3.30}$$

Using (3.27)–(3.28) into (3.30), the following expression is obtained

$$\begin{aligned} 6C\frac{dV}{dt} =& \text{sign}(v_{d1})(-2i_a v_{o_{a_z}} + i_b v_{o_{b_z}} + i_c v_{o_{c_z}} + \gamma_1) \\ &+ \text{sign}(v_{d2})(i_a v_{o_{a_z}} - 2i_b v_{o_{b_z}} + i_c v_{o_{c_z}} + \gamma_2) \\ &- 3x(\text{sign}(v_{d1})i_a + \text{sign}(v_{d2})i_b)\,. \end{aligned} \tag{3.31}$$

Hence, the proposed control law is to maximize the value of x when $(\text{sign}(v_{d1})i_a + \text{sign}(v_{d2})i_b) \geq 0$, and to minimize the value of x otherwise. In this regard, the maximization/minimization is limited by the achievable output voltage of the converter, which for a five level CHB converter is $v_{o_{i_z}} \in [-2,2]$—the lower limit is reached when both modules output their dc-link negatively, whereas the upper limit is reached when both modules output their dc-link positively. In other words, the control law for a five-level CHB converter clamps the output voltage of one phase to its upper/lower limit, and thus it is expressed as

$$\begin{aligned} &\text{if } (\text{sign}(v_{d1})i_a + \text{sign}(v_{d2})i_b) \leq 0 \\ &\quad x = -2 - \min(v_{o_{a_z}}, v_{o_{b_z}}, v_{o_{c_z}}) \\ &\text{else} \\ &\quad x = 2 - \max(v_{o_{a_z}}, v_{o_{b_z}}, v_{o_{c_z}})\,. \end{aligned} \tag{3.32}$$

As it was mentioned at the beginning of this section, this proposed law can be easily extended to CHB topologies with larger number of levels by considering the reachable voltage limits, which, in general terms, would be $v_{o_{i_z}} \in [-(N-1)/2, (N-1)/2]$ for a N-level converter.

3.2.2 Power boundaries obtention

In the following, it is derived how to obtain the power boundaries for the maximum difference between the total phase power consumption that grants that, when operating inside them, the current proposal makes the error signals v_{d1} and v_{d2} to stay around zero. For this, changes in the Lyapunov function value are no longer considered in continuous domain, but evaluated at the grid frequency rate (ω_g), resulting in a discrete modification of its value ΔV. In this way, the power limits that makes ΔV always negative when using the proposed control law are sought.

Assumptions

The power boundaries are obtained under steady-state conditions, therefore it is assumed that the dc-link and current controllers have reached the steady-state with unitary power factor conditions. This is equivalent to assuming that the phase currents and normalized voltage commands are sinusoidal as follows

$$i_a = A\cos(\omega_g t) \tag{3.33}$$

$$i_b = A\cos(\omega_g t - \frac{2\pi}{3}) \tag{3.34}$$

$$i_c = A\cos(\omega_g t + \frac{2\pi}{3}) \tag{3.35}$$

$$v_{o_{a_z}} = \frac{V_m}{\bar{v}_c^a}\cos(\omega_g t - \phi) = \frac{v_{o_a}}{\bar{v}_c^a} \tag{3.36}$$

$$v_{o_{b_z}} = \frac{V_m}{\bar{v}_c^b}\cos(\omega_g t - \frac{2\pi}{3} - \phi) = \frac{v_{o_b}}{\bar{v}_c^b} \tag{3.37}$$

$$v_{o_{c_z}} = \frac{V_m}{\bar{v}_c^c}\cos(\omega_g t + \frac{2\pi}{3} - \phi) = \frac{v_{o_c}}{\bar{v}_c^c}\ , \tag{3.38}$$

where A is the current amplitude, V_m is the amplitude of the voltage command, and ϕ stands for the phase-shift between modulated voltage and current.

Lastly, it is also assumed that the loads absorb a constant amount of power

$$I_c^a = \frac{p_a}{\bar{v}_c^a} \tag{3.39}$$

$$I_c^b = \frac{p_b}{\bar{v}_c^b} \tag{3.40}$$

$$I_c^c = \frac{p_c}{\bar{v}_c^c}\ , \tag{3.41}$$

where p_a, p_b and p_c are the absorbed power for each phase. Note that, for simplicity in the analysis, each phase power is expressed with one variable, although it does not exactly represent the total power consumption of the phase, as $\bar{v}_c^i \cdot I_c^i \neq v_{c1}^i I_{c1}^i + v_{c2}^i I_{c2}^i$ unless $v_{c1}^i = v_{c2}^i$. However, under steady-state conditions, the in-phase capacitor voltage unbalance regulation would make $v_{c1}^i = v_{c2}^i = \bar{v}_c^i$, and thus the previous generalization can be accepted.

Case analysis

Given that the signs of the error signals have been assumed constant in order to differentiate the Lyapunov function (3.29), there exist four cases that have to be analyzed individually. Introducing (3.33)–(3.41) into (3.31), and integrating over a grid period, where the signs of the error signals have been assumed, four inequalities are obtained to guarantee that $\Delta V < 0$. The four inequalities have the following expressions

$v_{d1} > 0, v_{d2} > 0$:

$$\int_0^{2\pi}\left(\frac{1}{\bar{v}_c^a}(p_a - i_a v_{o_a}) + \frac{1}{\bar{v}_c^b}(p_b - i_b v_{o_b}) - \frac{2}{\bar{v}_c^c}(p_c - i_c v_{o_c})\right)d\omega t < \int_0^{2\pi} 3x(i_a + i_b)d\omega t \tag{3.42}$$

$v_{d1} < 0, v_{d2} < 0$:

$$\int_0^{2\pi}\left(\frac{-1}{\bar{v}_c^a}(p_a - i_a v_{o_a}) - \frac{1}{\bar{v}_c^b}(p_b - i_b v_{o_b}) + \frac{2}{\bar{v}_c^c}(p_c - i_c v_{o_c})\right)d\omega t < \int_0^{2\pi} -3x(i_a + i_b)d\omega t \tag{3.43}$$

$v_{d1} > 0, v_{d2} < 0$:

$$\int_0^{2\pi} \left(\frac{3}{\bar{v}_c^a}(p_a - i_a v_{o_a}) - \frac{3}{\bar{v}_c^b}(p_b - i_b v_{o_b}) \right) d\omega t < \int_0^{2\pi} 3x(i_a - i_b) d\omega t \tag{3.44}$$

$v_{d1} < 0, v_{d2} > 0$:

$$\int_0^{2\pi} \left(\frac{-3}{\bar{v}_c^a}(p_a - i_a v_{o_a}) + \frac{3}{\bar{v}_c^b}(p_b - i_b v_{o_b}) \right) d\omega t < \int_0^{2\pi} -3x(i_a - i_b) d\omega t \,, \tag{3.45}$$

which, in order to simplify the analysis, are referred as

$$\int_0^{2\pi} H d\omega t < \int_0^{2\pi} F(x) d\omega t \,. \tag{3.46}$$

In the following, and in order to search for conservative power boundaries, the lower bound for $\int_0^{2\pi} F(x)$, and the upper bound for $\int_0^{2\pi} H$ are sought.

Lower bound for $F(x)$

Considering the behaviour of x given by the algorithm (3.32) and the current expressions given in (3.33)–(3.35), the minimum value of the integral of $F(x)$ can be computed as a function of the phase-shift angle ϕ and current amplitude A. In this regard, note that the integral of $F(x)$ in (3.42) and (3.43) would be equally bounded due to the fact that the sign of x changes with the sign of the error signals, and similarly happens with (3.44) and (3.45).

In this way, evaluating the integral for different values of ϕ, Fig. 3.6 is obtained. This figure shows the value of the integral for different values of ϕ, which results in the following conservative boundaries

$$\int_0^{2\pi} \pm 3x(i_a + i_b) d\omega t > 4.11 \cdot A \tag{3.47}$$

$$\int_0^{2\pi} \pm 3x(i_a - i_b) d\omega t > 7.13 \cdot A \tag{3.48}$$

Upper bound for H

To get the value of $\int_0^{2\pi} H d\omega t$, some additional assumptions are made from a conservative perspective. Firstly, the total power is denoted as p_t and fulfills $p_t = p_a + p_b + p_c$. Given that the currents and the voltage commands are sinusoidal and the systems performs with unitary power factor, the value of the integral $\int_0^{2\pi} i_i v_{o_i} d\omega t$ equals the total power shared between phases $p_t/3$.

Secondly, it is considered that it should exist a relation between the average capacitor voltage during the transient, where the capacitor voltages are unbalanced, and the power demanded by each phase. In the unbalanced transient and comparatively among phases, those with larger power demand would have a lower average capacitor voltage, whereas those with lower power demand would have a larger average capacitor voltage. Additionally, the error signals expresses whether an average capacitor voltage of a phase is above or below the averaged level (v_{dc}), e.g. $v_{d1} > 0$ indicates that the average capacitor voltage of phase a is below the average. Following this example and considering the previous assumption,

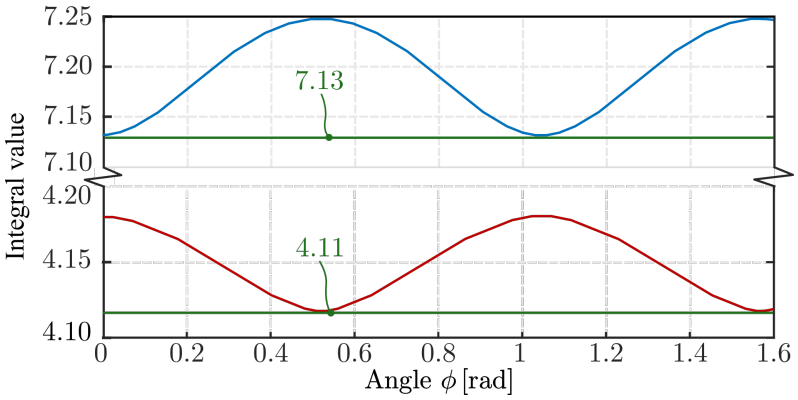

Figure 3.6 Value of the integral of $F(x)/A$ for different values of ϕ considering the sign of the error signals given in the inequalities (3.42) (lower curve) and (3.44) (upper curve). The values of the integral considering the sign of the error signals given in (3.43) and (3.45) depict the same waveform but shifted in phase, which gives the same lower boundaries.

phase a demands more power than the average, that is $p_a > p_t/3$. This assumption can be expressed in the following sets of inequalities depending on the signs of v_{d1} and v_{d2}

$$v_{d1} > 0, v_{d2} > 0: \quad p_a > \frac{p_t}{3}, p_b > \frac{p_t}{3}, p_c < \frac{p_t}{3} \tag{3.49}$$

$$v_{d1} > 0, v_{d2} < 0: \quad p_a > \frac{p_t}{3}, p_b < \frac{p_t}{3} \tag{3.50}$$

$$v_{d1} < 0, v_{d2} > 0: \quad p_a < \frac{p_t}{3}, p_b > \frac{p_t}{3} \tag{3.51}$$

$$v_{d1} < 0, v_{d2} < 0: \quad p_a < \frac{p_t}{3}, p_b < \frac{p_t}{3}, p_c > \frac{p_t}{3}\,. \tag{3.52}$$

Note that for the cases (3.50) and (3.51), the power demanded by phase c can not be directly related to the average consumption. Fortunately, the inequalities for those particular cases (3.44)–(3.45) do not require this information. Thanks to this, the terms that appear in the integral of H with the general expression of $\pm(p_i - i_i v_{o_i})$ are always positive under their assumption of error sign. For example, $v_{d1} > 0$ implies that $p_a > p_t/3$, and thus $(p_a - i_a v_{o_a}) > 0$.

Consequently, the upper bound of the integral of H can be obtained by maximizing all its terms since they are all positive when the previous assumptions are applied.

Another assumption involves imposing a constraint in the minimum allowed value of the average capacitor voltage for each phase ($\bar{v}_c^i$), as they appear in the denominator of the integral of H. Accordingly, this constraint—whose limit value is referred as $v_{c_{\min}}$—is determined as the value that allows modulating the grid voltage waveform without overmodulating. Assuming that the system works in rectifier mode—power inputs the system—with unitary power factor conditions, it is expected that the voltage command would be less or equal to the grid voltages. Hence, unitary modulation index results in a conservative assumption. Denoting the grid voltage rms value as V_{rms}, the constraint

results in $v_{c_{\text{min}}} = \sqrt{2}V_{\text{rms}}/2$. Using this value for $\bar{v}_c^a$, $\bar{v}_c^b$ and $\bar{v}_c^c$ in the integral of H given in (3.42)–(3.45), the following values are obtained

$$v_{d1} > 0, v_{d2} > 0: \quad \int_0^{2\pi} H d\omega t \geq \int_0^{2\pi} \frac{1}{v_{c_{\text{min}}}}(p_a + p_b - 2p_c) d\omega t \tag{3.53}$$

$$v_{d1} > 0, v_{d2} < 0: \quad \int_0^{2\pi} H d\omega t \geq \int_0^{2\pi} \frac{3}{v_{c_{\text{min}}}}(p_a - p_b) d\omega t \tag{3.54}$$

$$v_{d1} < 0, v_{d2} < 0: \quad \int_0^{2\pi} H d\omega t \geq \int_0^{2\pi} \frac{-1}{v_{c_{\text{min}}}}(p_a + p_b - 2p_c) d\omega t \tag{3.55}$$

$$v_{d1} < 0, v_{d2} > 0: \quad \int_0^{2\pi} H d\omega t \geq \int_0^{2\pi} \frac{-3}{v_{c_{\text{min}}}}(p_a - p_b) d\omega t\,, \tag{3.56}$$

which can be further simplified considering that $p_t = p_a + p_b + p_c$ and defining a relation parameter $r := p_b/p_t$

$$v_{d1} > 0, v_{d2} > 0: \quad \int_0^{2\pi} H d\omega t \geq \frac{2\pi}{v_{c_{\text{min}}}}(p_t - 3p_c) \tag{3.57}$$

$$v_{d1} > 0, v_{d2} < 0: \quad \int_0^{2\pi} H d\omega t \geq \frac{6\pi}{v_{c_{\text{min}}}}(p_t(1-2r) - p_c) \tag{3.58}$$

$$v_{d1} < 0, v_{d2} < 0: \quad \int_0^{2\pi} H d\omega t \geq \frac{-2\pi}{v_{c_{\text{min}}}}(p_t - 3p_c) \tag{3.59}$$

$$v_{d1} < 0, v_{d2} > 0: \quad \int_0^{2\pi} H d\omega t \geq \frac{-6\pi}{v_{c_{\text{min}}}}(p_t(1-2r) - p_c) \tag{3.60}$$

Power boundary obtention

Considering the integral limits of $F(x)$ in (3.47)–(3.48) and the integral limits of H in (3.57)–(3.60), a comparison can be performed. For this, the definition of total power with unitary power factor for a three-phase system with sinusoidal voltages and currents as $p_t = 3\frac{A}{\sqrt{2}}V_{\text{rms}}$ is considered. Considering the previous assumptions, the latter can be expressed as $p_t = 3Av_{c_{\text{min}}}$. As a result, the power boundaries as a function of the power consumed by phase c, total power p_t and the parameter r are obtained as follows

$$v_{d1} > 0, v_{d2} > 0: \quad p_c > 0.26p_t \tag{3.61}$$

$$v_{d1} > 0, v_{d2} < 0: \quad p_c > p_t(0.874 - 2r) \tag{3.62}$$

$$v_{d1} < 0, v_{d2} < 0: \quad p_c < 0.406p_t \tag{3.63}$$

$$v_{d1} < 0, v_{d2} > 0: \quad p_c < p_t(1.1261 - 2r) \tag{3.64}$$

These boundaries can be gathered together in a power region, inside which the algorithm is capable of keeping V_{d1} and V_{d2} around zero, no matter the sign of them. This power region is represented in Fig. 3.7 as a plane with the percentage of total power that is demanded by phase c as the vertical axis, and the percentage of the total power that is demanded by phase b—which is equal to $r \cdot 100$—in the horizontal axis.

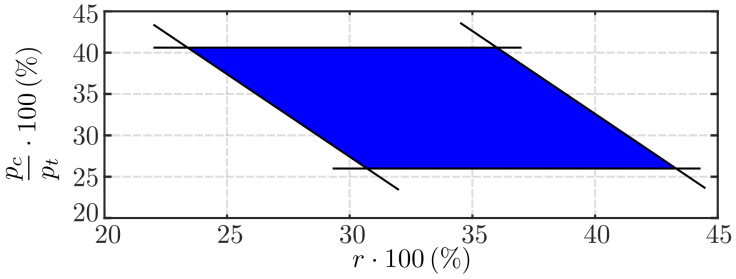

Figure 3.7 Region limited by the power boundaries obtained in (3.61)–(3.64).

3.2.3 Further improvement for neutral point voltage ripple

The previous algorithm computes the value of x in such a way that the voltage command of one phase is pushed to the limit of overmodulation, i.e. one $v_{o_{i_z}}$ is set to be -2 or 2. However, one of the most prominent application of CHBs is within the field of photovoltaic (PV) generation, and there exists a phenomenon with them that limits the ripple of the neutral point voltage. In PV, it has been shown that a parasitic capacitance appears between the neutral point of the converter and the ground, even when an isolation transformer is used in the PCC [176, 177]. Consequently, oscillations in the neutral point due to the injected zero-sequence voltage creates a current leakage that increases the losses. The larger the frequency and amplitude of the oscillations, the larger the losses.

During transients where the modules are not balanced, the sign of the error signals are kept constant, and thus the previous control law (3.32) generates a low-frequency oscillation—the value of x changes its sign at the grid frequency rate. However, when the system is reaching the steady-state condition, where the error signals can change abruptly, the frequency of the oscillations can considerably increase. If this is not taken into account, the neutral point voltage oscillations can reach frequencies close to the switching one, as the error signal sign can change from one sampling instant to another. In order to mitigate this effect during steady-state conditions, a modification of the previous control law is proposed in such a way that the amplitude of x is progressively reduced as the error signals get closer to their value at steady state

$$x_{\text{st}} \coloneqq K_x \cdot x\,, \quad K_x \in [0,1] \tag{3.65}$$

$$K_x = \text{Sat}(K_p(V - V^*))\,, \tag{3.66}$$

where x_{st} is the new proposed value of x to be added to the voltage commands, K_x is the factor that reduces the amplitude of x progressively, K_p is the control parameter that regulates K_x, and V^* is the value of the Lyapunov function around which it will stay at

steady state. Note that, due to the limitation of the original control law, the error signals would no longer oscillate around zero but around a fixed value dictated by V^*, and thus the abrupt changes of signs are avoided. As a consequence, the Lyapunov function is bounded in a band defined by the value of K_p and V^*. In this regard, note that the previous algorithm has been proved to make the error signals go to zero when it is fully applied and the phase powers are within the boundaries (3.61)–(3.64). Therefore, defining a band where (3.65) starts to reduce the value of x guarantees that the Lyapunov function is kept around this band, as the algorithm is fully applied outside its boundaries. This band can be obtained from considering the boundary value at which K_x equals 1

$$K_p(V_\mathrm{b} - V^*) = 1 \rightarrow V_\mathrm{b} = \frac{1}{K_p} + V^* \,,$$

where V_b is the Lyapunov function value at the limit of the band considered. Consequently, the value of V, when sampled at the grid frequency, is kept below V_b.

3.2.4 Simulation results

Some simulations have been carried out with the proposed control law and the modified one. For it, the system depicted in Fig. 3.5 is considered with the parameters shown in Table 3.1. The simulations implements a PI controller to regulate the average SM voltage towards its reference v_{dc}^* as the outer loop, whereas a PI controller in synchronous reference frame is used as the current controller (see Sect. 1.2.4). The output of the current controller is transformed back to the abc frame and the zero-sequence component computed by the proposed algorithm—or the modified version—is added. The resulting voltage command inputs the modulator that generates the gate signals.

Table 3.1 Simulation and control parameters.

Parameter	Value	Parameter	Value
SM volt. ref., v_{dc}^*	300 V	Phase a power, p_a	7 kW
Phase b power, p_b	5 kW	Phase c power, p_c	8 kW
Grid filter inductance, L_s	3.3 mH	Grid voltage, V_rms	220 $\mathrm{V_{rms}}$
SM capacitors, C	2 mF	Lyapunov ref., V^*	35
Prop. gain K_x regulation, K_p	0.1	Reactive power ref., q^*	0 VA
Switch. freq, f_s	10 kHz		

The simulations are conducted in the following intervals

1. The system starts with no loads and no zero-sequence injection until the current and dc-link voltage controllers reach a steady-state condition.
2. At $t = 0.35$ s, the constant power loads are activated, still with no zero-sequence injection.
3. At $t = 0.5$ s, the proposed algorithm is activated and the zero-sequence component is added to the voltage commands.

To depict the effect the proposed algorithm and its modification have on the capacitor voltage balance, Fig. 3.8 is depicted. It shows the evolution of the capacitor voltages and the error signals when the proposed control law and its modification are used. As it can be seen, both cases exhibit a capacitor voltage equalization tendency from the moment they are activated. However, in the case of the modified version, a steady-state error appears due to the limitation of the x value. Nevertheless, this error can be assumable in practical applications.

Similarly, Fig. 3.9 depicts the phase currents for the original algorithm. The phase currents for the modified algorithm are not shown as they exhibit a similar behaviour in steady state. As it can be seen, some low-order harmonics appear between $t = 0.35$ s and $t = 0.5$ s due to the modulation error caused by the capacitor unbalance. This distortion is further reduced when the algorithm is activated and the steady state is reached.

Lastly, Fig. 3.10 depicts the harmonic spectrum of the voltage between the neutral point of the converter and the ground. The values are depicted in normalized amplitude with regard to the fundamental amplitude (A_1). It can be seen that the inclusion of the modification considerably reduces the amplitude spectrum of higher frequencies, which would result in a lower leakage current.

3.2.5 Conclusions and future lines of research on CHB converters

The presented algorithm uses a well-known technique, that is the zero-sequence injection, to tackle the inter-phase capacitor unbalance in a five-level CHB converter. The proposed control law is computationally simple, and conservative limits for the phase power differences have been obtained inside which the algorithm is proved to provide balancing capabilities. A modification is later considered to make it more appealing for PV applications.

It is mentioned how the proposed control law could be extended to any CHB topology with different number of levels, however the power boundary analysis may require to be reformulated for the new converter. Nevertheless, the steps performed here can assist on the obtention of such boundaries.

Among the future lines of research, one can include the obtention of the instantaneous maximum deviation of the value of v_{d1} or v_{d2}, as the Lyapunov function reduction has been evaluated at the grid frequency rate. This means that the error signals could oscillate inside the grid period as long as, at the end of it, they have a lower value than the one they started with. Therefore, it may be necessary to perform an analysis to bound this ripple as it could generate undesired distortions. Another line could be the extension of this zero-sequence voltage injection to three-phase MMC.

Another possible future study is how this approach can be modified to additionally achieve negative sequence compensation in the phase currents.

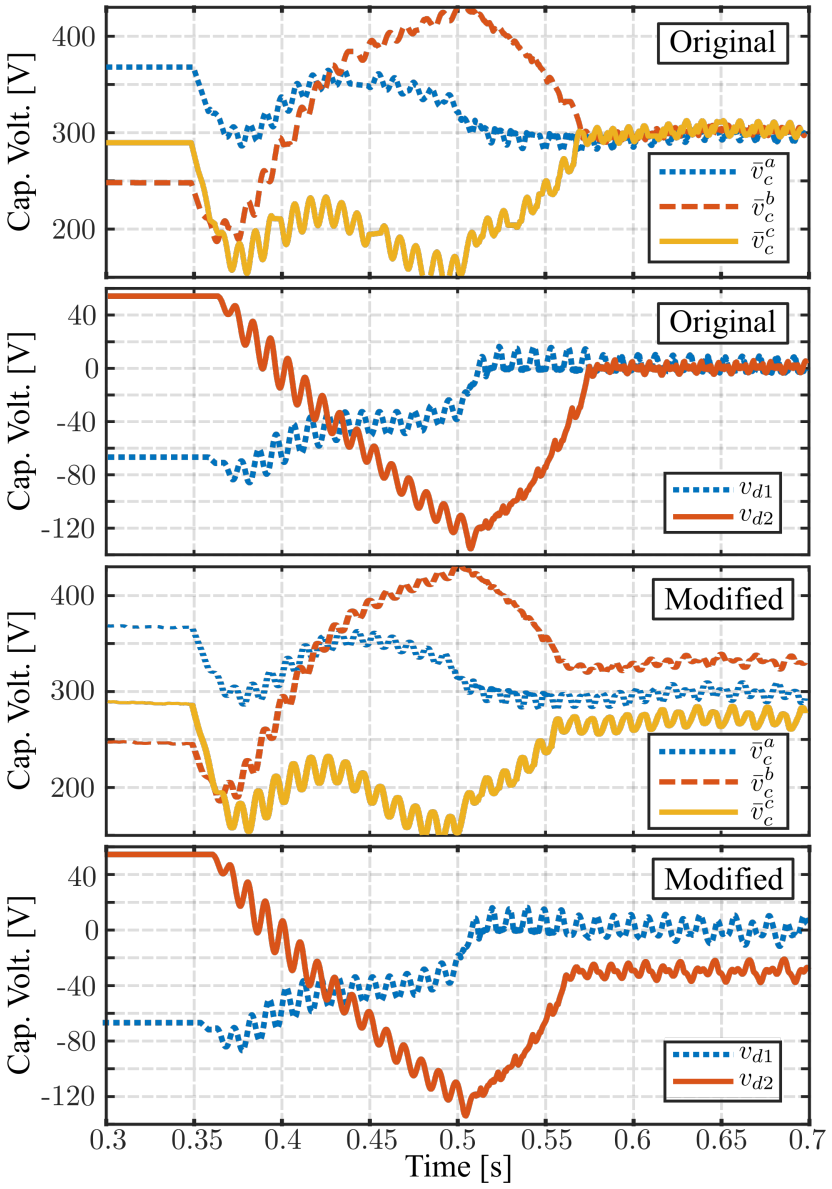

Figure 3.8 Evolution of the average capacitor voltage of each phase ($\bar{v}_c^a$, $\bar{v}_c^b$, $\bar{v}_c^c$) and the error signals (v_{d1}, v_{d2}) for the original algorithm and the modified one.

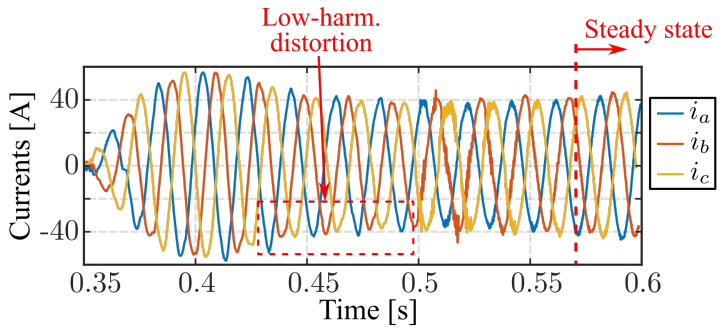

Figure 3.9 Evolution of the phase current from the moment the loads are activated with the inclusion of the original algorithm at $t = 0.5$ s.

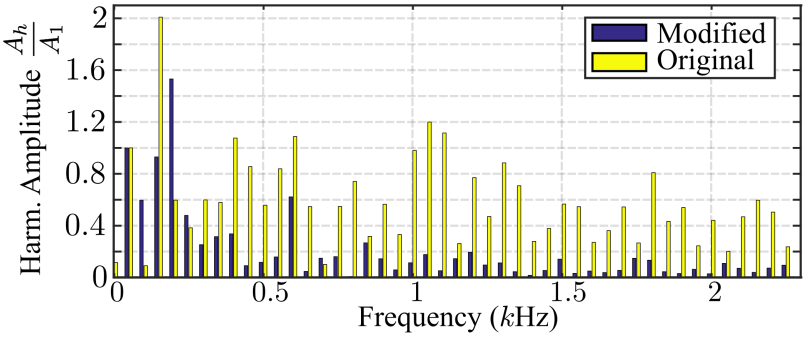

Figure 3.10 Harmonic spectrum of the voltage between the neutral point of the converter and the grid.

3.3 Feed-forward modulation technique for more accurate operation of MMC

This section exposes one contribution regarding the modulation of MMC [158] that achieves an improvement in the modulation accuracy of the system operation. The presented proposal is given for a single-phase MMC with N SMs per arm, but it can be extended to three-phase systems by applying the same procedure to the remaining phases. The system considered in this section is a single-phase MMC with half-bridge SMs shown in Fig. 3.11.

As it was mentioned in the introduction section of this chapter, the MMC stands out for its modularity, redundancy and scalability. Large voltage limits, that are unfeasible for two-level converters, can be reached by stacking modules with much more affordable voltage constrains, which makes this topology especially interesting for HVDC applications [178]. One way to approach the modulation of MMC is by dealing individually with each of the two arms that compose a phase (see Fig. 3.1) in such a way that each one has to fulfill a given voltage command. However, due to the fact that each module requires at least, one

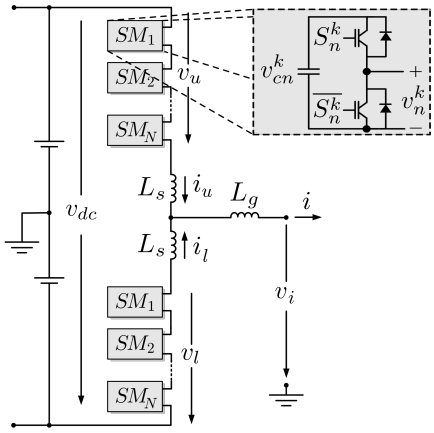

Figure 3.11 Scheme of a single-phase MMC with half-bridge SMs.

control signal, some efforts have been devoted to simplify the modulation stage once the voltage command is known. In this regard, the NLM achieves one of the best simplification along with low number of commutations. However, the loss of accuracy caused by selecting an integer number of SMs can generate distortions in the implemented controllers [179]. Alternatively, the use of PWM can compensate such inaccuracy [159, 160, 180]. Among others, PS-PWM [181] and LS-PWM [74] are the most used ones for a wide range of applications [182].

In any case, the voltage command of each arm is usually normalized, either considering the average voltage of the arm (indirect modulation) or the average voltage of the phase (direct modulation). Note that this step assumes that the SM voltage values are equal as the modulation makes no distinctions when selecting one SM or another. As a consequence, if the voltage difference between SMs is noticeable, a modulation error is produced. In the following section, the well-known NLM and LS-PWM approaches are recalled for a single-phase system and the stated modulation error is analytically exposed. An approach that compensates such modulation error is later proposed and exhibited in Sect. 3.3.2.

3.3.1 NLM and LS-PWM modulation approaches and problem statement

Given that the indirect modulation uses the average value of the SMs within the same arm ($\bar{v}_c^k$) for the normalization step, it achieves a more accurate operation. Therefore, in order to provide a fairer comparison with the proposal of this chapter, indirect modulation is used in the normalization step with LS-PWM and NLM approaches. For it, it is assumed that the voltage command for each arm—referred as v_k^* for arm $k = u,l$—are given as inputs, and then normalized resulting in the value of $v_{k_z}^* = v_k^*/\bar{v}_c^k$—sub-index $\square_z$ refers to normalized variable. Additionally, it is assumed that the control has reached the steady state, and thus the voltage commands are expected to have a sinusoidal shape.

To analyze the effects the equal capacitor voltage assumption has on the control accuracy, the control signal of the output current control (v_{dif} in (3.8)–(3.9) with the current dynamics

expressed in (3.2)) and the control signal of the circulating current control (v_{com} in (3.8)–(3.9) with the current dynamics expressed in (3.17)) are analyzed. In this regard, the voltage command for each arm determines a value that is later normalized and then introduced in the modulator. Then, the modulation error is the difference between the voltage command prior to the normalization and the real modulated voltage using the selected SMs.

NLM approach

This technique takes the normalized voltage command for each arm, and computes the rounded value to determine the number of connected SMs. Denoting n_u and n_l as the number of switched-on SMs in arm u and l respectively, the modulated voltage in the arm (v_k) can be derived as follows

$$\begin{cases} n_u & = \text{round}(v^*_{u_z}) \\ n_l & = \text{round}(v^*_{l_z}) \end{cases} ; \quad v_k = \sum_{n=1}^{n_k} v^k_{cn} \quad \text{for } k = u,l\,, \tag{3.67}$$

where v^k_{cn} is the capacitor voltage of the SM listed in the n^{th} position of the sorting algorithm, and round stands for the rounding function, which outputs the nearest integer. The value of $v^*_{k_z}$ is computed from the voltage command v^*_k and the average value of the capacitor voltage $\bar{v}^k_c$

$$v^*_{k_z} = v^*_k / \underbrace{\left(\frac{1}{N} \sum_{n=1}^{N} v^k_{cn} \right)}_{\bar{v}^k_c} \quad \text{for } k = u,l\,, v^*_{k_z} \in [0,N]\,. \tag{3.68}$$

With this, the actual arm voltage and the desired one can be compared and the modulation error ($\tilde{v}_k$) can be computed for each arm

$$\tilde{v}_u = v^*_u - v_u = \left(\frac{v^*_{u_z}}{N} - 1 \right) \sum_{n=1}^{n_u} v^u_{cn} + \frac{v^*_{u_z}}{N} \sum_{n=n_u+1}^{N} v^u_{cn} \tag{3.69}$$

$$\tilde{v}_l = v^*_l - v_l = \left(\frac{v^*_{l_z}}{N} - 1 \right) \sum_{n=1}^{n_l} v^l_{cn} + \frac{v^*_{l_z}}{N} \sum_{n=n_l+1}^{N} v^l_{cn}\,. \tag{3.70}$$

To give an illustrative example, Fig. 3.12 is depicted. Fig. 3.12(a) shows a capacitor voltage distribution of one arm for different values of N assuming $\bar{v}^k_c = v_{dc}$, whereas Fig. 3.12(b) depicts the modulation error described by (3.69)–(3.70) with the same capacitor voltage distribution for a generic arm k and different values of $v^*_{k_z} \in [0,N]$. It is worth mentioning that with this particular distribution, and knowing that $\bar{v}^k_c$ gets smaller with N, the larger the N, the smaller the error.

LS-PWM approach

The implementation of LS-PWM is equivalent to switching-on a number of SMs equal to the integer part of $v^*_{k_z}$, while the non-integer part is modulated by using PWM with one SM. Similarly than NLM, the n_k connected SMs are selected according to the sorting

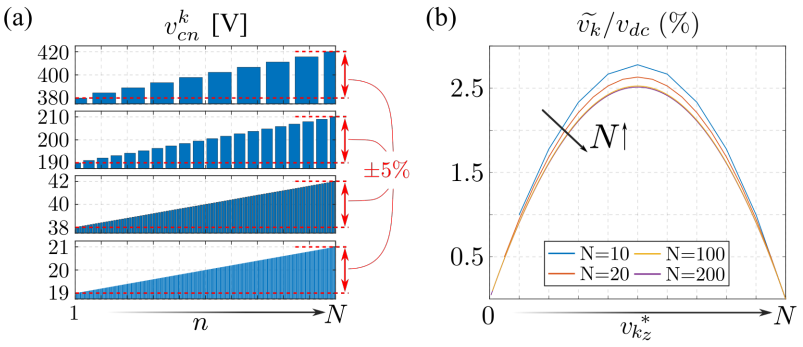

Figure 3.12 (a):Example of unequal capacitor voltage distribution with a maximum deviation of 5%; (b) Relative modulation error in one arm as a consequence of the unequal voltage values.

algorithm, being the $(n_k+1)^{\text{th}}$ in the list the one that is modulated through PWM. Thanks to this, the rounding error is compensated, but the assumption of equal capacitor voltage in the normalization step still takes place (3.68). Consequently,

$$\begin{cases} n_u &= \text{floor}(v_{u_z}^*) \\ n_l &= \text{floor}(v_{l_z}^*) \end{cases} ; \quad v_k = \sum_{n=1}^{n_k} v_{cn}^k + d_{n_k+1}^k v_{cn_k+1}^k \quad \text{for } k = u,l \,, \tag{3.71}$$

where $d_{n_k+1}^k \in [0,1]$ is the duty ratio of the PWM-switched SM. From this notation, the error for LS-PWM can be modelled as

$$\tilde{v}_u = \left(\frac{v_{u_z}^*}{N} - 1\right) \sum_{n=1}^{n_u} v_{cn}^u + \frac{v_{u_z}^*}{N} \sum_{n=n_u+1}^{N} v_{cn}^u - d_{n_u+1}^u v_{cn_u+1}^u \,, \tag{3.72}$$

$$\tilde{v}_l = \left(\frac{v_{l_z}^*}{N} - 1\right) \sum_{n=1}^{n_l} v_{cn}^l + \frac{v_{l_z}^*}{N} \sum_{n=n_l+1}^{N} v_{cn}^l - d_{n_l+1}^l v_{cn_l+1}^l \,, \tag{3.73}$$

which differs from the NLM expressions (3.69)–(3.70) in the last duty ratio term.

In order to depict the modulation error that is produced by both approaches, Fig. 3.13 is shown. This figure illustrates the value of v_k for different values of N when the capacitor voltage distribution of Fig. 3.12(a) is considered. As it can be seen, the modulation error is generally reduced for larger number of SMs (N). Additionally, it is clear that the greater the capacitor voltage differences, the larger the error induced by the normalization step. For this, it is desired to find an approach that solves this issue, which will be of great interest for applications with relatively low number of SMs and large expected differences in the capacitor voltages. Accordingly, the potential applications for this approach will be discussed later.

To provide a numerical example for LS-PWM, consider $N = 10$, $\bar{v}_c^k = 200$ V, $v_k^* = 650$ V, and a random capacitor voltage distribution with a 10 % maximum allowed deviation

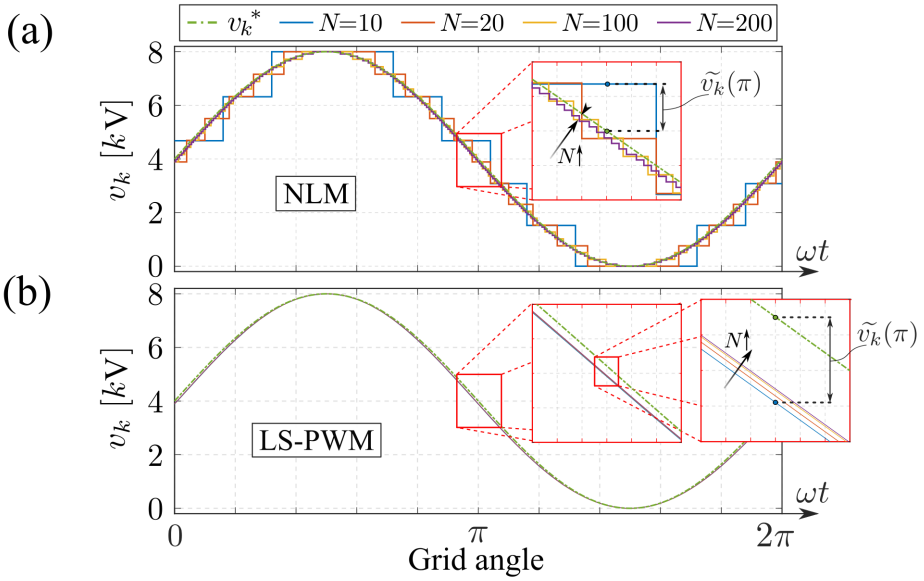

Figure 3.13 Example of modulated arm voltage over a grid period using NLM (a) and LS-PWM (b) for different values of N with the capacitor voltage distribution of Fig. 3.12.

that are listed from lower to higher as follows

$$
\begin{aligned}
v_{cn}^{k} &= [180,188,190,195,\ldots] \\
v_{k_z}^{*} &= \frac{650}{200} = 3.25
\end{aligned}
$$

Using LS-PWM: (3.74)

$$
\begin{aligned}
n_k &= 3, \quad d_4^k = 0.25 \\
v_k &= 180 + 188 + 190 + 195 \cdot 0.25 = 606.75\,\mathrm{V} \\
\tilde{v}_k &= 650 - 606.75 = 43.25\,\mathrm{V}\,(6.6\%\ \text{error})\,,
\end{aligned}
$$

where a deviation of a 6.6 % from the desired value is given. This value would change depending on the capacitor voltage distribution and the value of $v_{k_z}^*$, affecting in any case the closed-loop performance of the controllers.

3.3.2 Feed-forward LS-PWM approach (FF-LS-PWM)

This is the main contribution of this section [158], and it consists of a modulation technique that solves the mentioned modulation issue by taking into account the actual capacitor voltage of the connected SMs. For it, the desired arm voltage v_k^* is considered, and the SMs are stacked from the sorting algorithm list until their added voltage matches v_k^*. Similarly to LS-PWM, there is one SM that is PWM-switched in each arm, and thus a

more accurate modulation is achieved. Due to the use of the capacitor voltage values and the same principle of operation than LS-PWM, this proposal is called feed-forward LS-PWM (FF-LS-PWM).

The concept of feed-forward modulation is not new as it was already presented in [183] for space-vector-based modulation for multilevel converters. However, the current proposal adapts it to MMC using a much more simple CB-PWM. A similar concept of feed-forward modulation for MMC was introduced in [168], where the authors use PS-PWM and a voltage command for each SM. In this way, the normalization step is carried out for each individual SM, and its capacitor voltage value is taken into account in the duty ratio computation. However, due to the use of PS-PWM and the use of individual voltage commands, a large computational effort is expected along with large switching losses as all SMs are PWM-switched. On the contrary, the proposed approach makes, for each arm, simple comparisons to derive the number of connected SMs, and one normalization to obtain the corresponding duty ratio. Using variable j as a counter, this process can be sequenced as follows

1. Variable v_k^* is saved into variable v_{k1}^*.
2. Starting with $j=1$, variable v_{kj}^* is compared with the j^{th} SM in the sorted algorithm list—let us denote it as $v_{cn_j}^k$. If v_{kj}^* is larger, then the respective SM is fully connected, i.e. $d_{n_j}^k = 1$, and the algorithm continues with the next step. Otherwise, the respective SM is PWM-switched with $d_{n_j}^k = v_{kj}^*/v_{cn_j}^k$, the remaining SMs, i.e. SM_n for $n = j+1,\ldots,N$, are disconnected ($d_{n_j}^k = 0$), and the algorithm ends.
3. If the previous SM was fully connected, the variable j is updated $j = j+1$.
4. The remaining arm voltage to be modulated is then updated considering the previous decision, that is $v_{kj}^* = v_{kj-1}^* - v_{cn_{j-1}}^k$, and the process is repeated again from point (2).

This process ends with the computation of the PWM-switched SM, similarly to the LS-PWM, where the last selected SM in the sorted list is the PWM-switched one. The proposed process is depicted in Fig. 3.14 along with an illustrative example.

Note that the current proposal can be seen as a modification of the carriers for LS-PWM. Following in this line, the carriers would not be normalized from 0 to 1, but instead they would go from zero to $v_{cn_j}^k$. Additionally, the disposition of the carriers can be configured similarly to that of a LS-PWM (see Sect. 1.3.2) in such a way that the benefits derived from it are obtained. Following this concept of altering the carriers to achieve feed-forward modulation in MMC, the PS-PWM scheme could also be applied to derive a FF-PS-PWM. In this case, each carrier is phase-shifted $360/N$ similarly to PS-PWM, but its amplitude is modified according to the capacitor voltage value of the SM the carrier is associated with. Larger values of the SM capacitor voltage implies a shorter conduction time to achieve the same average value of the modulated voltage. Note that a typical scheme of PS-PWM uses the normalized voltage command and the carriers go from zero to N. Therefore, a linear relation can be implemented to take into account the capacitor voltage value in the carriers amplitude, that is, going from zero to Nv_{cn}^k instead. As a result, the carriers in PS-PWM no longer have a triangular waveform that goes from zero to N and then back to zero,

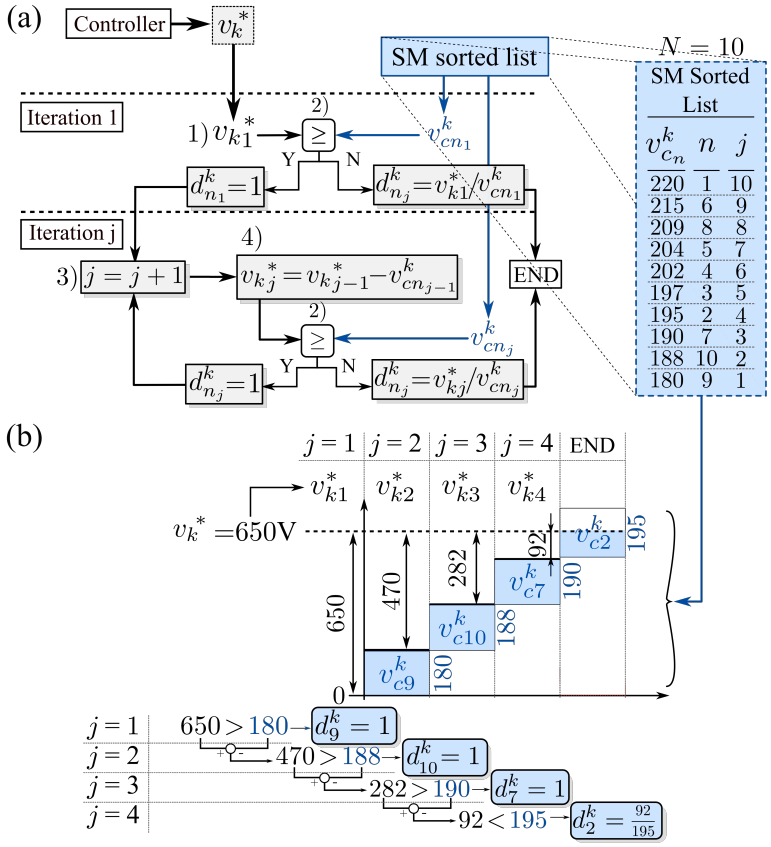

Figure 3.14 (a) Flowchart of proposed modulation approach. (b) Example of proposed modulation for $N = 10$, a given sorted list and $v_k^* = 650V$.

instead they go from zero to Nv_{cn}^k and back to zero. To depict an illustrative example, the schemes of FF-LS-PWM and FF-PS-PWM implemented through carriers are shown in Fig. 3.15 for a MMC with five modules.

3.3.3 Analysis and discussion

This section provides a theoretical analysis of the proposed method in comparison with NLM and LS-PWM in order to exhibit the error compensation achieved by the proposal. For this, $N = 20$ is assumed and the SM capacitor voltages are normalized ($v_{cn_z}^k$) (with respect to $\bar{v}_c^k$) and distributed as depicted in Fig. 3.16. This analysis considers a maximum deviation of 30%, i.e. $v_{cn_z}^k \in [0.7,1.3]$, and that the SMs are already arranged by the sorting algorithm in the proper order, $n = 1,\ldots,20$. Furthermore, a sinusoidal reference $v_{k_z}^*$ with

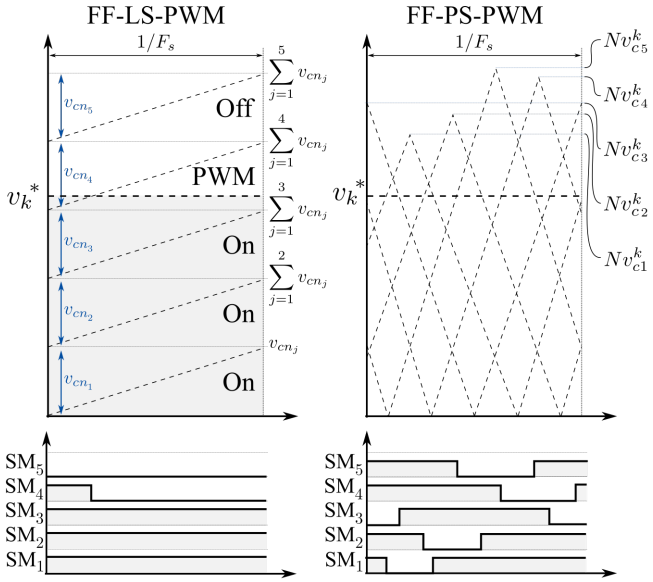

Figure 3.15 Implementation of the feed-forward concept in the carriers for LS-PWM and PS-PWM with five SMs.

unity modulation index is assumed. Expressing the above considerations mathematically

$$v_{cn_z}^u(n) = 1 - 0.3\sin((n-10)\frac{\pi}{20}) \tag{3.75}$$

$$v_{cn_z}^l(n) = 1 + 0.3\sin((n-10)\frac{\pi}{20}) \tag{3.76}$$

$$v_{u_z}^* = -10\cos(\omega t) + 10 \tag{3.77}$$

$$v_{l_z}^* = 10\cos(\omega t) + 10 \tag{3.78}$$

$$v_{\text{dif}_z}^* = v_{l_z}^* - v_{u_z}^* \tag{3.79}$$

$$v_{\text{com}_z}^* = v_{l_z}^* + v_{u_z}^* = 20, \tag{3.80}$$

where $v_{\text{dif}_z}^*$ is the normalized voltage command for the output current controller (see Eq. (3.8)–(3.9)), and $v_{cn_z}^k(n)$ refers to the continuous function that expresses the n-capacitor voltage for arm k. Using the continuous function with the averaged model of NLM and LS-PWM to obtain the normalized modulated voltage v_{dif_z}

$$v_{\text{dif}_z} = v_{l\,z} - v_{u\,z} \tag{3.81}$$

$$\text{NLM: } v_{\text{dif}_z} = \underbrace{\int_0^{\text{round}(v_{l_z}^*)} v_{cn_z}^l(n)dn}_{v_{l\,z}} - \underbrace{\int_0^{\text{round}(v_{u_z}^*)} v_{cn_z}^u(n)dn}_{v_{u\,z}} \tag{3.82}$$

$$\text{LS-PWM: } v_{\text{dif}_z} = \underbrace{\int_0^{v_{l_z}^*} v_{cn_z}^l(n)dn}_{v_{l_z}} - \underbrace{\int_0^{v_{u_z}^*} v_{cn_z}^u(n)dn}_{v_{u_z}}. \tag{3.83}$$

With this, the modulated voltage v_{dif_z} can be compared with the corresponding voltage command v_{dif}^* as portrayed in Fig. 3.17. It can be seen that the modulation error generates DC and low-order harmonics in the modulation of v_{dif_z}, which will ultimately impact the performance of the converter.

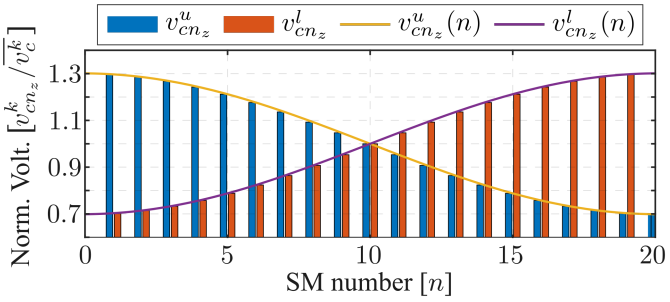

Figure 3.16 Normalized capacitor voltage distribution used for the analysis with $N = 20$, and the continuous function that interpolates them.

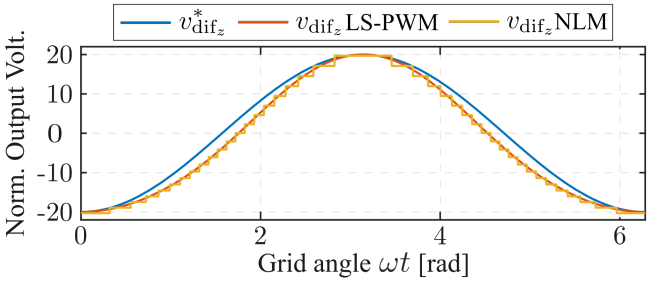

Figure 3.17 Normalized output voltage for NLM and LS-PWM versus the desired one, considering the continuous function of the capacitor voltage values of Fig. 3.16.

A similar procedure can be carried out for the modulation of $v_{\text{com}_z}^*$, that is, the control variable for the circulating current (Eq. 3.16). Accordingly,

$$v_{\text{com}_z} = v_{l_z} + v_{u_z} \tag{3.84}$$

$$\text{NLM: } v_{\text{com}_z} = \underbrace{\int_0^{\text{round}(v_{l_z}^*)} v_{cn_z}^l(n)dn}_{v_{l_z}} + \underbrace{\int_0^{\text{round}(v_{u_z}^*)} v_{cn_z}^u(n)dn}_{v_{u_z}} \tag{3.85}$$

$$\text{LS-PWM: } v_{\text{com}_z} = \underbrace{\int_0^{v^*_{l_z}} v^l_{cn_z}(n)dn}_{v_{l_z}} + \underbrace{\int_0^{v^*_{u_z}} v^u_{cn_z}(n)dn}_{v_{u_z}}. \tag{3.86}$$

However, in order to assume the worst case scenario for v_{com_z}, that is the distribution of capacitor voltages that yields the highest error, it is assumed that both arms share the same continuous function of capacitor voltages, i.e. $v^u_{cn_z}(n) = v^l_{cn_z}(n)$. This is due to the fact that the particular waveforms of Eq. (3.75)–(3.76) would generate no modulation error in the common component. The modulated voltage v_{com_z} can be compared with the commanded one $v^*_{\text{com}_z}$ (3.80) as portrayed in Fig. 3.18, where it can be seen that undesired components at twice the fundamental component could arise in the circulating current.

As a result of this analysis, it is stated that LS-PWM and NLM have a modulation inaccuracy that might force the controller to supplement such an error, imposing additional restrictions on the controller design, or even generating instabilities as this error can be seen as external disturbance in the closed-loop scheme. With the FF-LS-PWM scheme, these modulation errors are avoided and an accurate modulation is achieved.

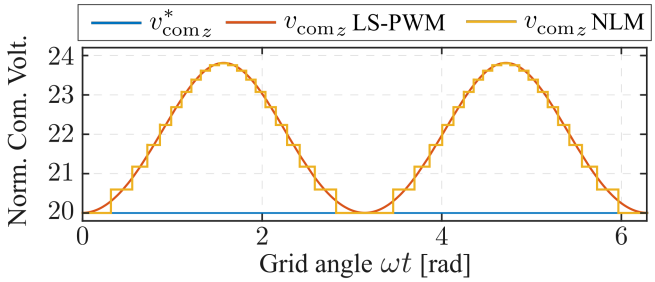

Figure 3.18 Normalized common voltage for NLM and LS-PWM versus the desired one, considering that both arms share the same continuous function of the capacitor voltage shown in Fig. 3.16.

Despite the benefits of the current approach, the feedforward concept requires measuring every capacitor voltage value every switching period, which could be a deterrent feature for systems with large number of SMs. In fact, some efforts have been devoted to reduce the sampling frequency required for MMC, especially in the capacitor voltage measurements [184–186]. Additionally, the considered algorithm compares the voltage command with the capacitor voltage values one by one, which might be of concern in terms of computational burden in systems with large values of N. Nevertheless, there are several practical applications where the mentioned drawbacks are largely compensated by the derived benefits from using FF-LS-PWM. Examples include:

- Solutions to medium- or low-voltage applications [187], where the number of SMs is relatively low and the capacitor voltage differences are more remarkable. In these scenarios, the added complexity is kept low due to the reduced number of measures, while the achieved modulation error compensation enhances the system performance.

- Integrating renewable energies [188], and energy storage systems [189]. Naturally, these applications result in unequal steady-state SM capacitor voltages and/or uneven power consumption among SM. This is the case of the application exhibited in Sect. 2.3.4 for five-level DCC.
- Application of switching reduction or switching-saving approaches (SSA) [190], which are evolving with MMC as an attempt to reduce losses and increase efficiency. One way to achieve it is by prolonging the conduction time of SMs, which in turns increases the difference between SMs capacitor voltages. Due to this, SSAs will be considered in the simulation and experimental verification to exhibit one of the potential application of this approach.
- Using smaller capacitors to enable a more compact MMC system [191]. This can be achieved by relaxing the permissible capacitor voltage ripple [192], which would compromise the quality and the performance of the system were the actual capacitor voltage not to be taken into account in the modulation stage.

3.3.4 Simulation results

This section depicts some results obtained from simulating the proposed method in comparison with LS-PWM. Direct comparison with NLM is skipped given that the literature is plenty of comparisons between LS-PWM and NLM, and that LS-PWM performs better than NLM in terms of accuracy.

The system is a single-phase MMC inverter in grid-forming application, where the output (point i in Fig. 3.11) is connected to a load (R_L) of 10 Ω. The control scheme is the one shown in Fig. 3.3 and Fig. 3.4, which was extracted from [168], where the output current control is a proportional-resonant controller (Sect. 1.2.4) that tracks a fixed current reference with amplitude $I^* = 32\,A$.

In order to verify the improvement of FF-LS-PWM against LS-PWM when the capacitor voltage differences are noticeable, a SSA that is based on relaxing the allowable capacitor voltage difference is used. The fundamental of such algorithm is to avoid fast changes of the SM positions in the sorting algorithm list when steady state is reached, as every change in the sorting algorithm list usually implies the connection/disconnection of a previously disconnected/connected SM. As a result, if the position of a SM in the sorting algorithm list is not updated until its voltage reaches a certain deviation from the reference value, it would remain connected/disconnected for longer period of time, saving commutations in the process. Consequently, the SM stays connected/disconnected until their capacitor voltage reaches the boundaries of the band, moment at which its connection priority is updated and its voltage change tendency is modified favourably. For the remaining of this simulation section, the voltage band is set to be 5% of the capacitor voltage reference $v_c^* = v_{dc}/N$, which is fixed to 50 V for all tests. Consequently, the dc-link voltage varies accordingly with N as $v_{dc} = 50 \cdot N$ V. Besides, the control parameters and current reference are kept constant between tests to provide a fairer comparison.

The first test shows the circulating current behaviour for LS-PWM and FF-LS-PWM for different number of SMs (N) in Fig. 3.19. Note how the FF-LS-PWM improves the controllability and smooths the current distortion due to the improved modulation accuracy.

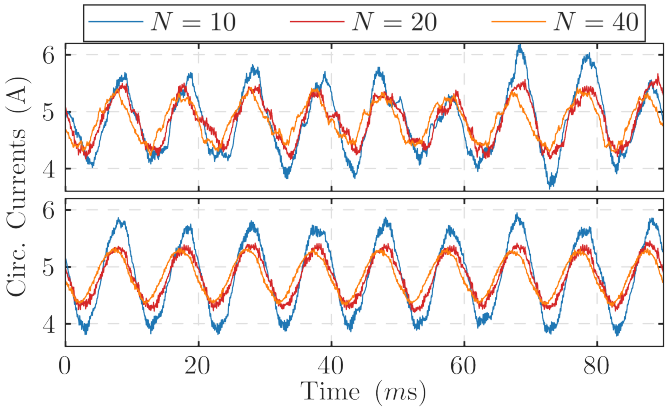

Figure 3.19 Circulating current for LS-PWM (top) and FF-LS-PWM (bottom) with a SSA with a voltage band of 5%, for different values of N.

To exhibit the effect the capacitor voltage differences have on the output current distortion, Fig. 3.20 depicts the THD value of the output current under different values of N for LS-PWM and FF-LS-PWM with and without the voltage-based SSA. As it can be seen, considering that $\bar{v}_c^*$ is fixed, the modulation error increases with the number of SMs when a SSA is used. However, FF-LS-PWM is capable of compensating such modulation error, resulting in small variations of the THD value. Besides, the use of SSA while adopting FF-LS-PWM has a negligible effect on the THD value. With a switching and sampling frequency of 5 kHz, the average SM switching frequency that results from LS-PWM and FF-LS-PWM with and without SSA are shown in Table 3.2. Note that both modulations yield similar switching performance, but the distortion is improved with FF-LS-PWM, especially when SSA is used.

Table 3.2 Average f_s (kHz) per SM obtained from simulation.

N	LS-PWM	FF-LS-PWM	LS-PWM (SSA)	FF-LS-PWM (SSA)
20	3.05	3.03	0.96	0.95
40	3.82	3.79	0.85	0.85
80	4.28	4.28	0.76	0.76
150	4.40	4.39	0.72	0.72
200	4.47	4.44	0.71	0.71

In summary from this section, it can be extracted that FF-LS-PWM with SSA exhibits a slightly better distortion performance with considerable reduced commutations when compared with LS-PWM without SSA. LS-PWM with SSA achieves a similar switching reduction at the expenses of largely worsening the distortion performance. It is worth mentioning that PS-PWM in [168] could present an improvement in the current distortion, but it will be at the cost of PWM-switching every SM, and increasing the computational burden due to the duty ratio computation for each SM.

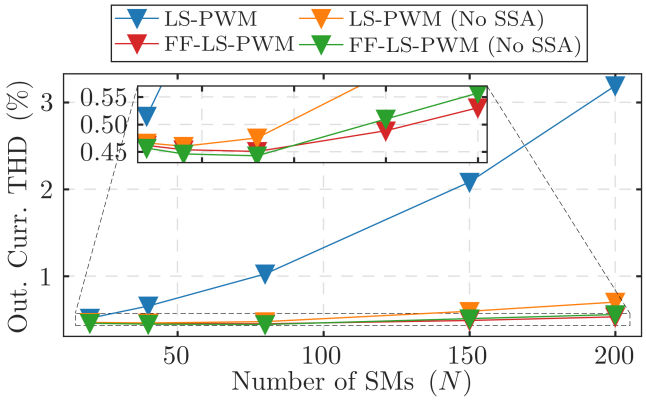

Figure 3.20 THD value of the output current for LS-PWM and FF-LS-PWM when the number of SMs are increased.

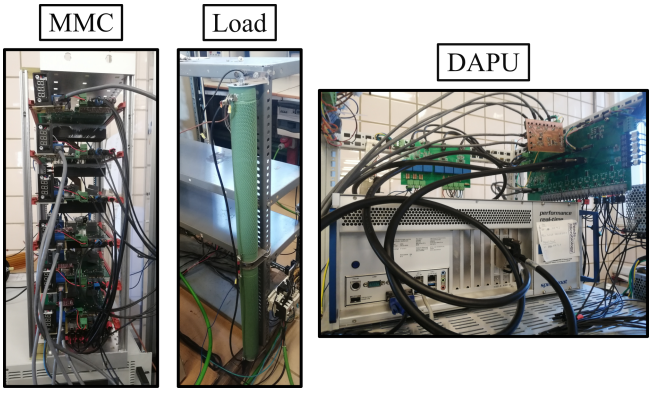

Figure 3.21 Single-phase MMC used in experiments along with data acquisition and processing unit (DAPU) and external resistor used as load.

3.3.5 Experimental verification

This section provides some experiments to verify the feasibility of the proposal. For this, a 200 W scaled-down single-phase laboratory prototype is used (Fig. 3.21). This setup of a MMC has 6 modules, three per arm. The parameters of the experimental set-rig are tabulated in Table 3.3. The used control scheme is the same than the one used in simulations, and depicted in Fig. 3.3 and Fig. 3.4. The control parameters K_p^{PI} and K_i^{PI} are used for the PI controller of the average capacitor voltage ($\bar{v}_c \rightarrow v_c^* = v_{dc}/N$); K_p^{P} are used either for the P controller of the circulating current ($i_{\text{circ}} \rightarrow i_{\text{circ}}^*$) and the balance of the capacitor voltages between arms ($\bar{v}_c^u \leftrightarrow \bar{v}_c^l$); whereas K_p^{PR} and K_r^{PR} are the control parameters of the resonant controller used for the output current.

In this experimental verification, different scenarios of SSA with LS-PWM and FF-LS-PWM are considered. The first one is based on a voltage band as explained in the

Table 3.3 Experimental parameters.

Parameter	Value	Parameter	Value
Arm Inductance, L_s	2 mH	Output Inductance, L_g	2 mH
SM Capacitance, C_{SM}	2 mF	Number of SM per arm, N	3
Load Resistance, R_L	60 Ω	Load Current reference, I^*	1 A
dc-link Voltage, v_{dc}	150 V	Samp. and switch. Freq., f_s	10 kHz
Output frequency	50 Hz	Prop. avg. cap., K_p^{PI}	0.1
Int. avg. cap., K_i^{PI}	0.05	Prop. circ. curr. and bal., K_p^{P}	1
Prop. Out. Curr., K_p^{PR}	20	Res. Out. Curr., K_r^{PR}	500

simulation section, and the second one uses a time counter [193], which updates the sorting list when a given time has elapsed. The aim of this is to prolong the conduction time of each SM, and hence reducing the switching events at the cost of generating larger voltage ripple. This SSA will be referred as the counter-based one and it will be associated with a time counter value.

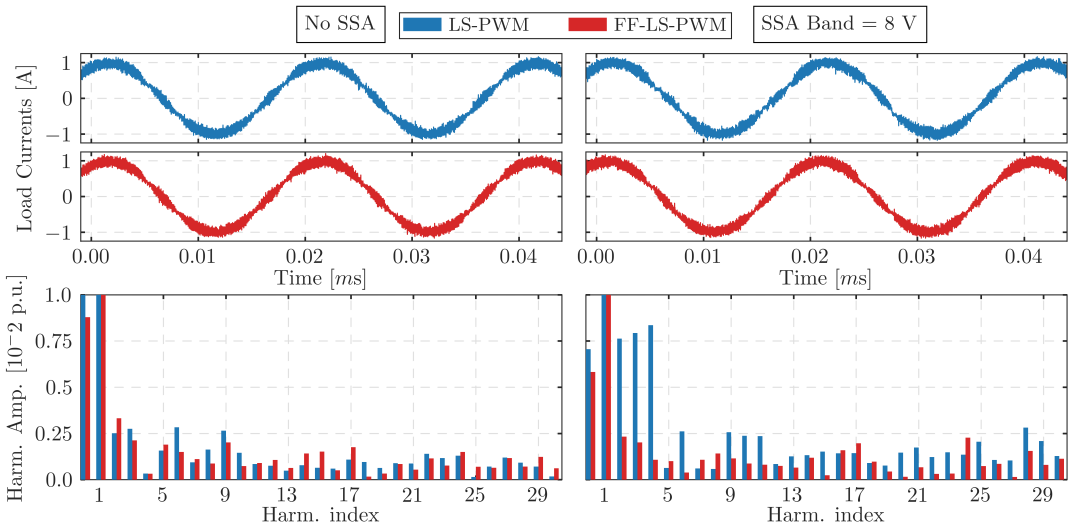

Figure 3.22 Experiment results: Load current and its harmonic spectrum for the LS-PWM and the FF-LS-PWM when no SSA and SSA with voltage band of 8 volts are considered.

The first evaluated variable is the load current (i) for the LS-PWM and the FF-LS-PWM with and without SSA, which is depicted in Fig. 3.22 along with its low-order harmonic spectrum. Both approaches exhibit similar performance when SSA is not applied. However, low-order harmonics appear in LS-PWM when the SSA is implemented. In contrast, with FF-LS-PWM the harmonic profile remains unchanged. In terms of circulating current, the error associated with the use of SSA affects the stability of the current control, causing

loss of controllability at some instants. This is obviously clear from Fig. 3.23, where the circulating currents for LS-PWM and FF-LS-PWM under different switching frequencies are depicted.

A similar consequence can be seen in Fig. 3.24, where the load currents with fundamental frequency of 100 and 200 Hz, and the circulating currents of FF-LS-PWM and LS-PWM are shown. This test was performed with a SSA with a voltage band of 8 V.

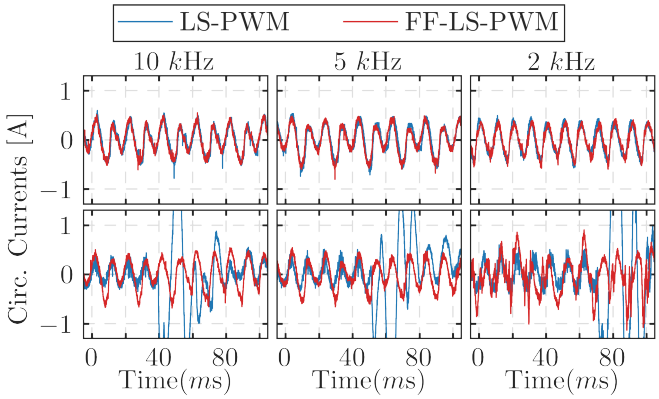

Figure 3.23 Circulating current of the LS-PWM and the FF-LS-PWM under different switching frequencies (10, 5 and 2 kHz) when no SSA (top) and SSA with a voltage band of 8 V (bottom) are considered.

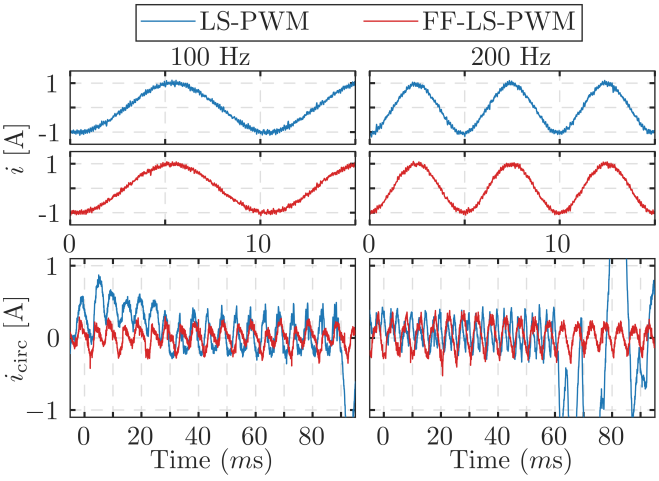

Figure 3.24 Load and circulating currents when modulating 100 and 200 Hz output signals for the LS-PWM and the FF-LS-PWM while using a SSA with a voltage band of 8 V.

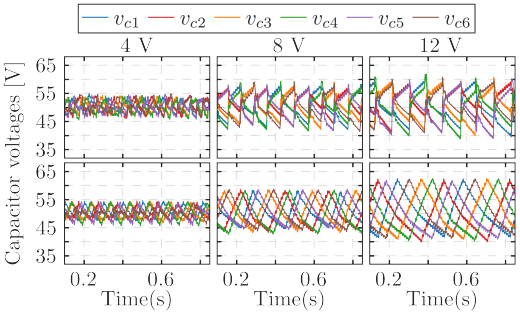

Figure 3.25 Capacitor voltage evolution of the SMs for the LS-PWM (top) and the FF-LS-PWM (bottom) when voltage-based SSA is used under different values of the voltage band.

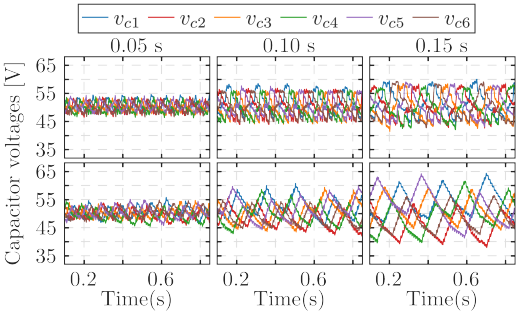

Figure 3.26 Capacitor voltage evolution of the SMs for the LS-PWM (top) and the FF-LS-PWM (bottom) when counter-based SSA is used under different values of the time counter.

Additionally, Fig. 3.25 and 3.26 demonstrate how the capacitor voltages evolve under both SSAs. Note that, in spite of exhibiting large differences between SMs, FF-LS-PWM achieves a more linear evolution in the capacitor voltages due to the fact that the balancing closed-loop is not affected.

Extensive experimental testing were conducted on LS-PWM and FF-LS-PWM, looking into different performance indices as summarized in Table 3.4. These include: total harmonic distortion (THD) of the load current; harmonic distortion of the first 40 harmonics ($\text{HD}_{[0-40]}$) of the load current—to indicate the low-order harmonic presence—; the average switching frequency of all SMs ($\bar{f}_s$)—measured and computed over 70 fundamental periods—, and the standard deviation (σ_{f_s}) of the six SM switching frequencies. With this, the benefits of FF-LS-PWM in achieving overall better THD values and lower low-order harmonic contents over all considered SSA scenarios are exhibited. Moreover, the proposed FF-LS-PWM improves the commutation reduction achieved by the SSA, regardless of the method used. Also note that the value of σ_{f_s} in the FF-LS-PWM, when applying SSA with low values of voltage band or time counter, is lower than the LS-PWM while still achieving a reduction in the number of commutations. This could suggest the feasibility of using FF-LS-PWM with SSA to reduce the switching losses and to equalize the SM usage as the average switching frequencies tend to be closer in value.

It is shown how the proposal performs under different capacitor voltage difference profiles using two different techniques of SSA. However, other approaches that require relaxed capacitor voltage difference constraints between SMs within the same arm would be benefited from using FF-LS-PWM.

3.3.6 Conclusions and future lines of research on MMC

This proposal addresses the error resulted from the normalization step of typical modulations for MMC. It has been exhibited that ignoring the capacitor voltage ripple in the

Table 3.4 Summary of experimental results.

SSA	THD [% A/A_1]		$HD_{[0-40]}$ [% A/A_1]		Avg. swt. freq. f_s [kHz]		σ_{f_s} [Hz]	
	LS-PWM	FF-LS-PWM	LS-PWM	FF-LS-PWM	LS-PWM	FF-LS-PWM	LS-PWM	FF-LS-PWM
No SSA	11.77	11.87 [+1%]	1.45	1.43 [-1%]	7.705	7.724 [0%]	11.3	11.6 [+3%]
Band 4	12.01	11.87 [-1%]	1.31	1.20 [-8%]	6.815	6.725 [-1.3%]	11.5	9.04 [-21%]
Band 8	12.18	11.42 [-6%]	2.60	1.13 [-56%]	6.996	6.732 [-3.8%]	9.32	21.2 [+127%]
Band 12	13.31	11.64 [-13%]	5.12	1.15 [-78%]	7.047	6.732 [-4.5%]	9.96	26.9 [+170%]
Counter 0.05	11.85	11.96 [+1%]	1.86	1.93 [+4%]	6.763	6.731 [-0.5%]	10.2	5.25 [-49%]
Counter 0.10	11.92	11.79 [-1%]	2.41	1.89 [-22%]	6.852	6.729 [-1.8%]	22.4	14.1 [-37%]
Counter 0.15	12.76	11.72 [-8%]	4.48	1.27 [-72%]	6.917	6.728 [-2.7%]	23.2	27.3 [+18%]

modulation stage results in an error that has a negative impact in the system performance, especially in applications where the capacitor voltage differences are large. The proposed FF-LS-PWM solves the latter by taking into account the reference voltage and the individual capacitor voltages of each SM. Hence, an accurate arm voltage modulation is achieved.

The FF-LS-PWM is tested experimentally and compared with the standard LS-PWM while using a switching-saving algorithm. The results show that FF-LS-PWM does not increase the THD value of the output current while the capacitor voltage values can move around a band up to $\pm 24\%$, at the same time that a 13% of commutation reduction is achieved. In contrast, LS-PWM suffers from these differences, compromising the performance of the implemented controllers, which is avoided by the introduction of FF-LS-PWM.

The theoretical analysis supported by simulation and experimental verification showed the feasibility and effectiveness of the proposed approach. Finally, it is worth mentioning that the accuracy achieved comes at the expenses of increased computational requirement associated with the instantaneous measurement of the SM capacitors. However, the gained benefits outweigh these challenges, especially with the advancement in digital processing technologies, where intelligent approaches can be easily incorporated.

Among the possible future lines of research are:

1. The use of the feed-forward concept with predictive models to estimate the capacitor voltage value of each SM, in such a way that the required sampling frequency is reduced.
2. The incorporation of the feed-forward concept to three-phase systems with other modulation approaches, such as predictive NLM.
3. A guide to select reduced capacitors by taking advantage of the FF-LS-PWM performance. This will include examining the safety ripple limits and designing strategies that guarantee safe operation while using FF-LS-PWM.

4 Conclusions

The most important thing is to keep the most important thing the most important thing.

DONALD P. CODUTO

The present work introduces some principles of the power electronic field. In this regard, this paper revisits the basic principles of power converters, with special focus on grid-connected voltage source converters, their common controllers and the most well-known modulation algorithms. Later on, some well-known techniques to address synchronization and compensation under unbalanced grid operation are presented and theoretically compared. Given that the main contributions framework is within the field of multilevel converters, some of the most common topologies and their necessity of addressing additional control objectives are shown, along with some modulation and control algorithms that tackle their increased control complexity.

In the following, the particular contributions of this work and possible future works related to them are mentioned.

4.1 Particular Contributions of this work

Once the multilevel converter topology has been introduced and their control problem has been stated, most of this work devotes to the development and research of one particular topology: the diode-clamped converter. In this line, the three-level (NPC) and five-level (5-L DCC) topologies were the principal targets of the carried-out research.

Regarding the three-level topology, a hybrid dynamical system formulation is revisited, which was modelled taking into account the hybrid nature of the converter. In such a work, a hybrid control law is formulated and later proved to guarantee UGAS under the design operating point. The contribution involves the integration of the control law in a real grid-connected power converter, which required the modification of some control parameters to compensate for non-modelled dynamics. Additionally, a modification of the control

law is proposed in such a way that the benefits of using a three-level topology are further exploded without spoiling the UGAS guarantee that was established in the theoretical framework. The carried-out experiments prove the feasibility of such a proposal.

Most of the contributions of this work lie in the five-level DCC topology. Firstly, a previously presented integrated control and modulation algorithm that tackles the capacitor voltage balance in the control stage, rather than the modulation one, is revisited. Then, a modification is proposed that reduces the switching losses and improves the harmonic performance, as it is later shown in simulation and validated through experiments. A further analysis of these integrated controllers, both the original and the modified one, is developed from a thermal perspective in another proposal. As a result, some comparative conclusions about the conducting losses of each proposal are derived. Afterwards, using the same modelling than the integrated controller, the control schemes are reformulated in a proposal for an application that involves individual solar cell arrays connected to each capacitor of the dc-link. With this, the dc-dc stage is skipped and the MPPT for each individual solar array is fulfilled, which improves the overall efficiency of the system.

On a different line of research inside five-level DCCs, a previously presented mixed-integer optimization approach for determination of the modulation criteria is recalled. Given that the online resolution of such optimization problem is unfeasible, two approaches are sequentially presented:

- Online implementation through LUTs. For this, the optimization problem is solved offline for a working operating conditions, and the resulting modulation criteria are stored in look-up tables for later use during online operation. This approach is validated through simulations and experiments, along with some steps for a robust integration. Besides, it is also compared with other well-known modulation approaches and the mentioned integrated controller, exhibiting noticeable improvements in terms of distortion and balancing capabilities.
- Training and using CARTs based on the optimization problem formulation. This approach comes as a solution for the lack of flexibility of the previous proposal. This approach revisits the original problem formulation, adding some criteria to look for a more beneficial solution, and then it is solved for several operating points. With this, several CARTs are trained and the resulting decision trees are used for online operation. The approach is validated and compared by simulations and experiments, along with some rules for a robust integration. As a result, and thanks to the generalization capability of CARTs, a more flexible solution is obtained, whose range of operation can reach points that were not covered in the training set, as it is shown both in experiments and simulations. Additionally, it is also compared with the LUT-based approach and the same approaches that were used for comparison in the work of the LUT-based algorithm, exhibiting enhanced performance and wider range of operating points.

Additionally, in the field of multilevel converter, Chap. 3 is focused on providing solutions related to the capacitor voltage balance for cascaded H-bridge converters and modular multilevel converters. Firstly, these two topologies are presented and their principle of operation are exhibited. For the CHB, a simple algorithm that uses the zero-sequence injection is proposed to address the capacitor voltage balance between phases when different

power consumption in the phases is given. This algorithm is analyzed and conservative power boundaries, inside which its balancing capabilities are probed, are derived. Besides, some carried-out simulations verify its good behaviour.

For the MMC, the modulation error caused by assuming the capacitor voltages of the SMs to be equal prior to the modulation stage when using NLM and LS-PWM is exposed. Some discussion and analysis are presented for both approaches, and an alternative, based on LS-PWM, is presented. With this, the modulation error is corrected, and an improvement in the controllability and phase current distortion is achieved. It is also exhibited that the latter is more remarkable when compared with the standard LS-PWM in applications with large capacitor voltage differences, such as those that use SSA. As a result, SSA can be used, while the downsides of having larger capacitor voltage differences are neglected. This approach is compared and tested through simulation, and validated with experiments.

4.2 Future work

Apart from the future works that are exposed at the end of each contribution, the following lines of research could be considered

- The use of hybrid dynamical system to model unbalances in the grid, mainly negative and positive sequence components. With this, an hybrid control law could be derived for distorted grid voltages either to assist on the correction of it, or to guarantee the injection of positive-sequenced currents.
- The derivation of a model that takes into account the effect that unbalanced capacitor voltages, in multilevel converters, have on the modulation performance and its interaction with a weak grid. It could be of interest the search of certain working conditions that assists on the weak grid restoration or compensates the grid unbalances to inject balanced currents.
- The use of the dc-link capacitors in multilevel converters to address other particular applications. The proposed application of the integrated control and modulation for solar arrays is an example that could be considered in this line, but with the addition of experimental verification. Besides, other topologies could be considered, such as MMC with the proposed feed-forward modulation and solar arrays connected to each SM. Furthermore, battery management and interface with smart grids could be included.

List of Figures

List of Tables

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